DGT304RE13

Gate Turn-off Thyristor

Replaces DS5518-3.0 DS5518-4 July 2014 (LN31738)

FEATURES

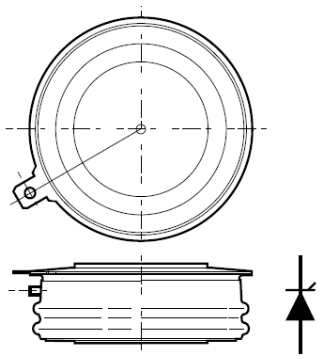
- Double Side Cooling
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- High Surge Current Capability
- Turn-off Capability Allows Reduction in Equipment Size and Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements

APPLICATIONS

- Variable speed AC motor drive inverters (VSD-AC)
- Uninterruptable Power Supplies
- High Voltage Converters
- Choppers
- Welding
- Induction Heating
- DC/DC Converters

KEY PARAMETERS

V_{DRM}	**1300V**
$I_{T(AV)}$	**250**
I_{TCM}	**700A**
dV_D/dt	**500V/µs**
dI_T/dt	**500A/µs**



Outline type code: E

(See Package Details for further information)

Fig. 1 Package outline

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} (V)	Repetitive Peak Reverse Voltage V_{RRM} (V)	Conditions
DGT304RE13	1300	1300	T_{vj} = 125°C, I_{DM} =50mA, I_{RRM} = 50mA, V_{RG}=2V

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	V_D = 60%V_{DRM}, T_j = 125°C, dI_{GQ}/dt = 15A/µs, C_S = 2.0 µF	700	A
$I_{T(AV)}$	Mean on-state current	T_{HS} = 80°C, Double side cooled. Half sine 50Hz	250	A
$I_{T(RMS)}$	RMS on-state current	T_{HS} = 80°C, Double side cooled. Half sine 50Hz	390	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non repetitive) on-state current	10ms half sine. T_j = 125°C	4.0	kA
I^2t	I^2t for fusing	10ms half sine. T_j = 125°C	80	kA^2s
di_T/dt	Critical rate of rise of on-state current	V_D =60% V_{DRM}, I_T = 700A, T_j = 125°C, I_{FG} > 20A, Rise time > 1.0 μs	500	A/μs
dV_D/dt	Rate of rise of off-state voltage	To 80% V_{DRM}; R_{GK} ≤ 1.5Ω, T_j = 125°C	500	V/μs

GATE RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value may be exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		-	50	A
$P_{FG(AV)}$	Average forward gate power		-	10	W
P_{RGM}	Peak reverse gate power		-	6	kW
di_{GQ}/dt	Rate of rise of reverse gate current		10	50	A/μs
$t_{ON(min)}$	Minimum permissible on time		20	-	μs
$t_{OFF(min)}$	Minimum permissible off time		40	-	μs

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-hs)}$	Thermal resistance – junction to heatsink surface	Double side cooled	DC	-	0.075	°C/W
		Single side cooled	Anode DC	-	0.12	°C/W
			Cathode DC	-	0.20	°C/W
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 6.0kN With mounting compound	Per contact	-	0.018	°C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	125	°C
T_{OP}/T_{stg}	Operating junction/storage temperature range			-40	125	°C
F_m	Clamping force			5.0	6.0	kN

CHARACTERISTICS

T_j = 125°C unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{TM}	On-state voltage	At 600A peak, $I_{G(ON)}$ = 2A dc	-	2.2	V
I_{DM}	Peak off-state current	V_{DRM} = 2500V, V_{RG} = 0V	-	25	mA
I_{RRM}	Peak reverse current	At V_{RRM}	-	50	mA
V_{GT}	Gate trigger voltage	V_D = 24V, I_T = 100A, T_j = 25°C	-	0.9	V
I_{GT}	Gate trigger current	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.0	A
I_{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	50	mA
E_{ON}	Turn-on energy	V_D = 900V, I_T = 600A, dI_T/dt = 300A/µs I_{FG} = 20A, rise time < 1.0µs Residual inductance, R_L = 3µH	-	130	mJ
t_d	Delay time		-	1.5	µs
t_r	Rise time			3.0	µs
E_{OFF}	Turn-off energy	I_T = 600A, V_{DM} = 750V, Snubber capacitor C_S = 1.5µF, di_{GQ}/dt = 15A/µs Residual inductance, R_L = 3µH	-	350	mJ
t_{gs}	Storage time		-	11	µs
t_{gf}	Fall time		-	0.9	µs
t_{gq}	Gate controlled turn-off time		-	11.9	µs
Q_{GQ}	Turn-off gate charge			700	µC
Q_{GQT}	Total turn-off gate charge			1400	µC

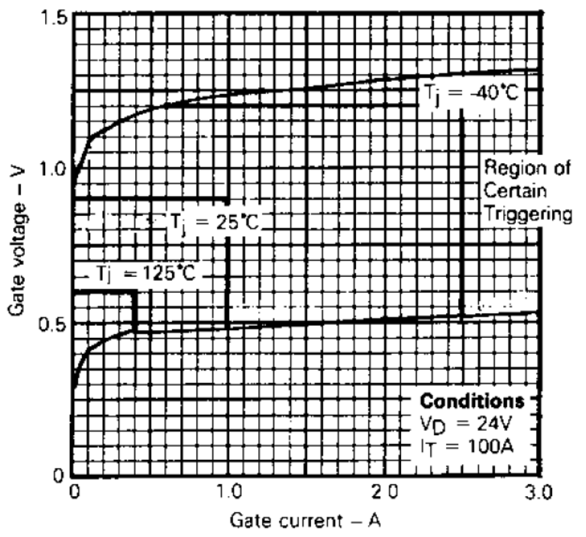


Fig.2 Gate Characteristics

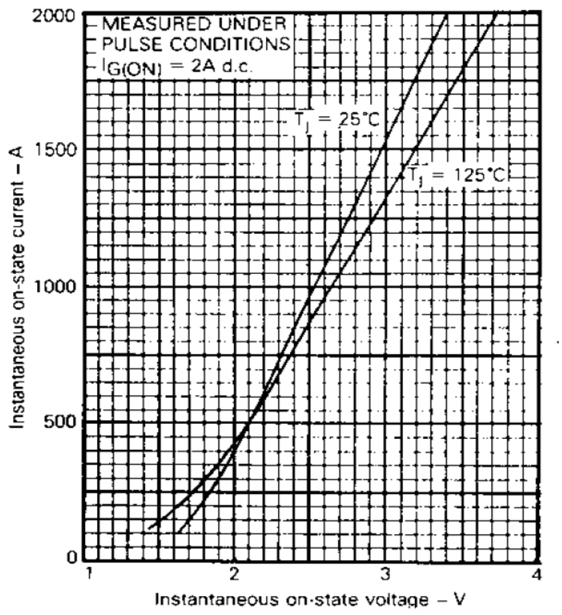


Fig.3 On-state characteristics

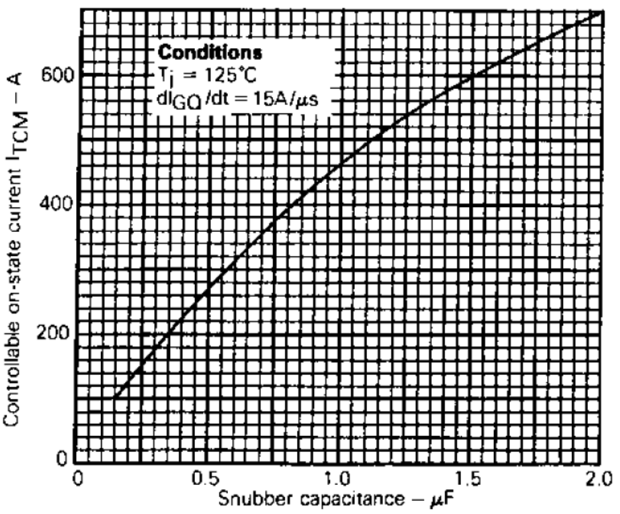


Fig.4 Maximum dependence of I_{TCM} on C_S

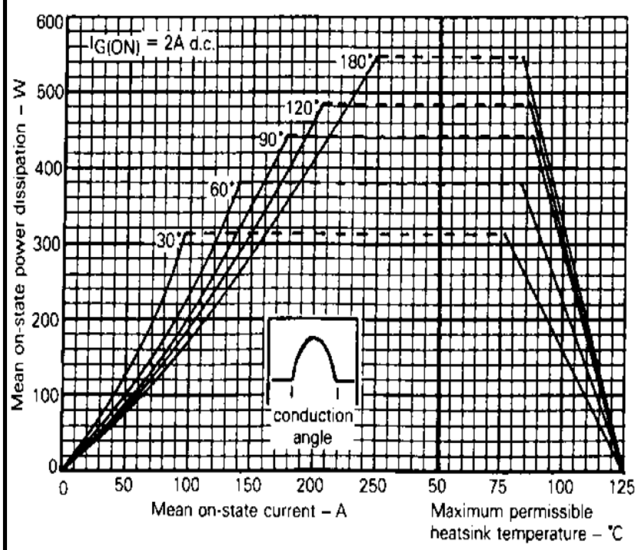


Fig.5 Steady state sinusoidal wave conduction loss – double side cooled

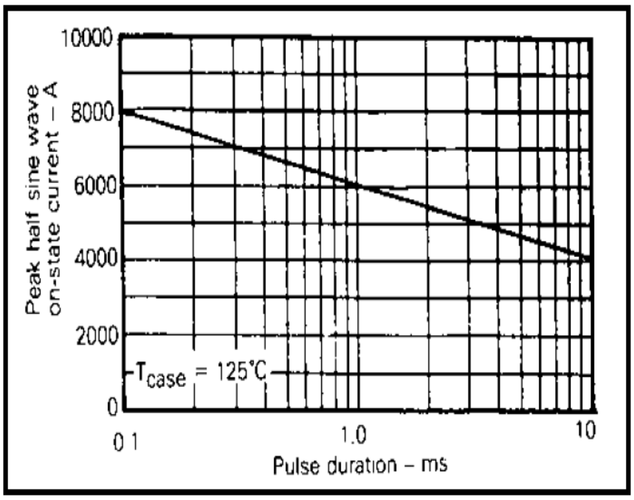


Fig.5 Surge (non-repetitive) on-state current vs time

Fig.6 Surge (non-repetitive) on-state current vs time

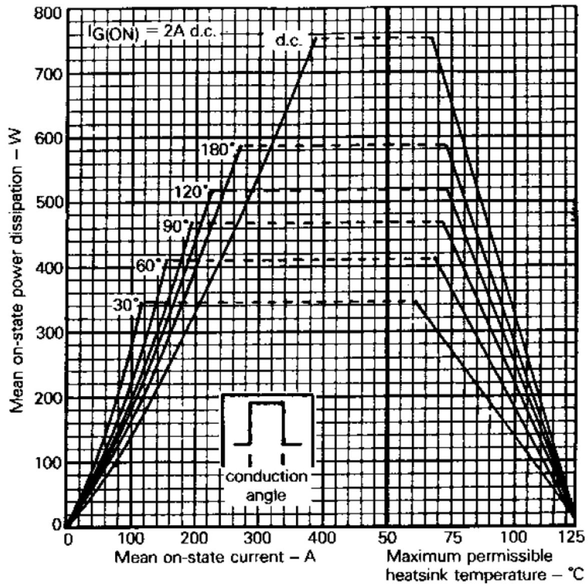


Fig.7 Steady state rectangular wave conduction loss – double side cooled

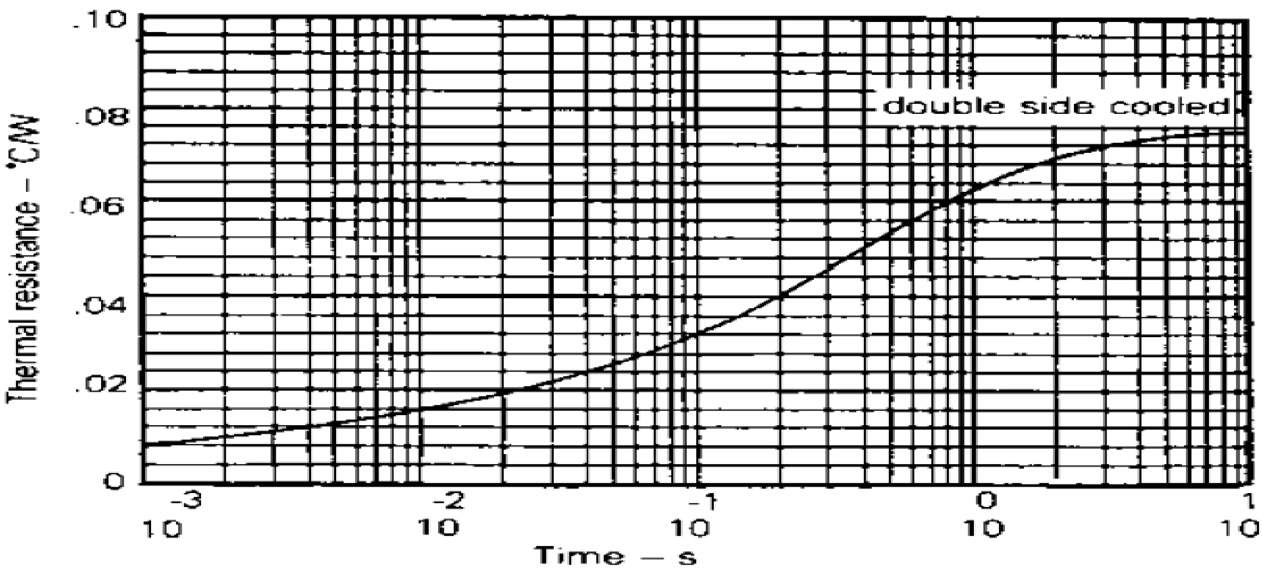


Fig.8 Maximum (limit) transient thermal impedance – junction to case (°C/kW) double side cooled

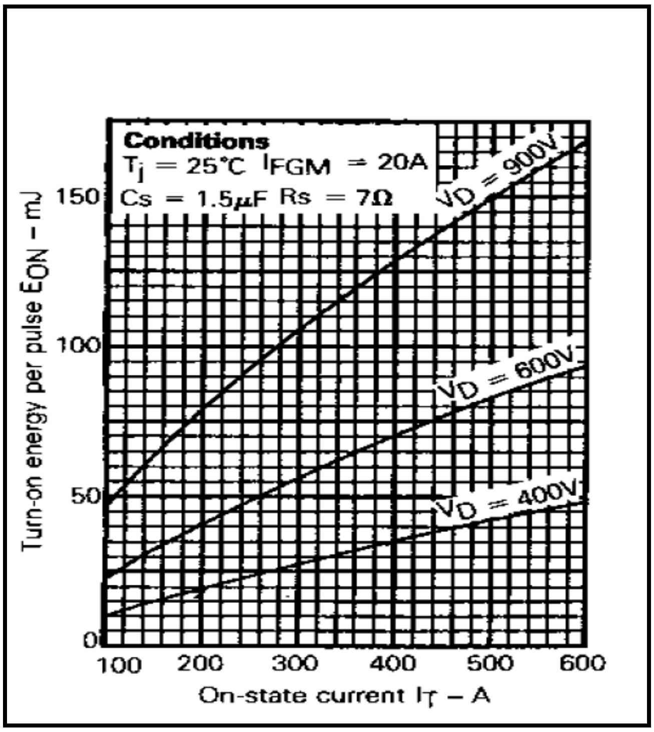


Fig.9 Turn-on energy vs on-state current

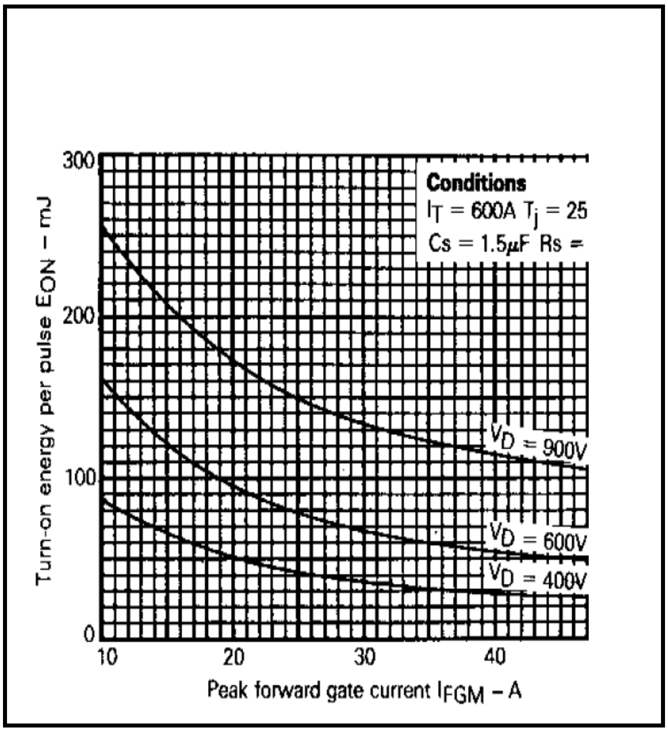


Fig.10 Turn-on energy vs peak forward gate current

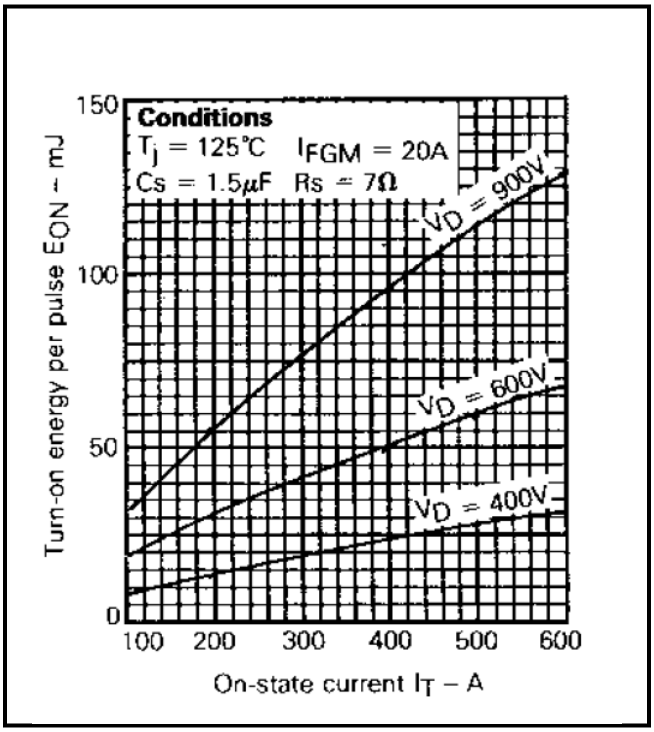


Fig.11 Turn-on energy vs on-state current

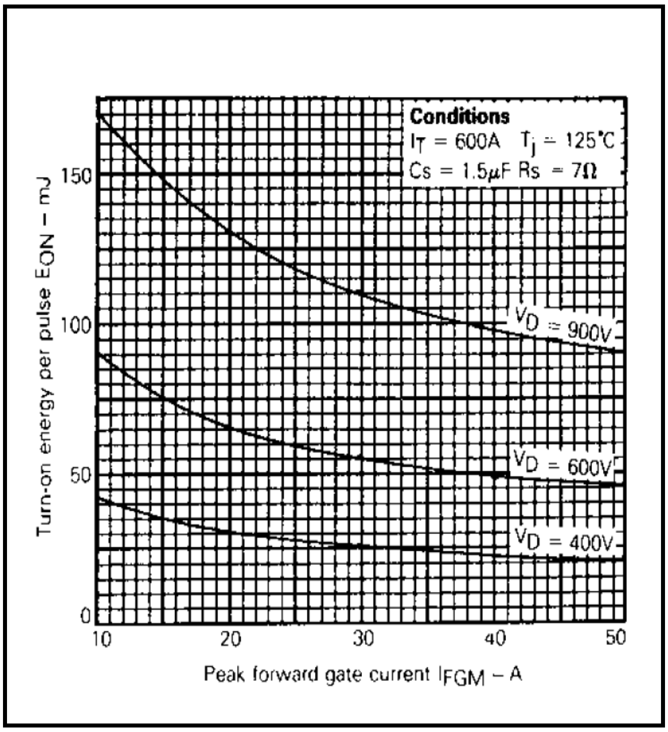
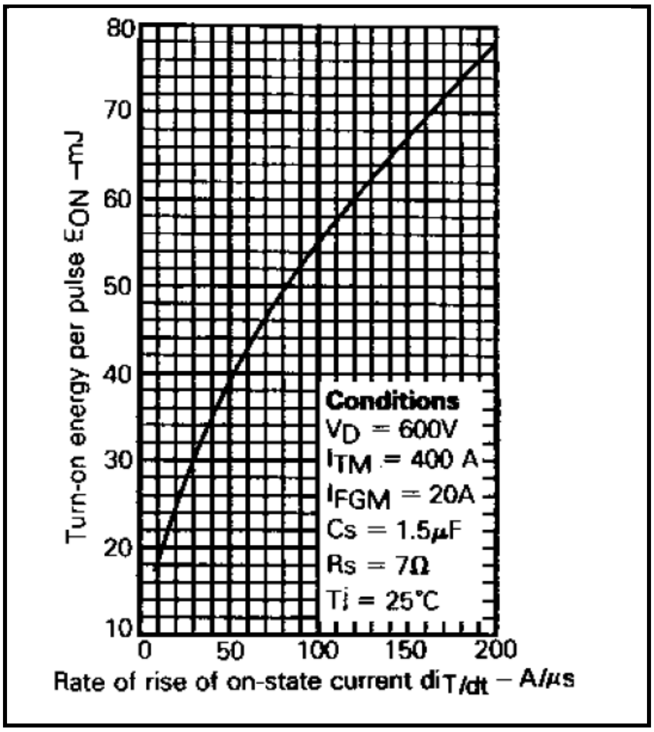


Fig.12 Turn-on energy vs peak forward gate current



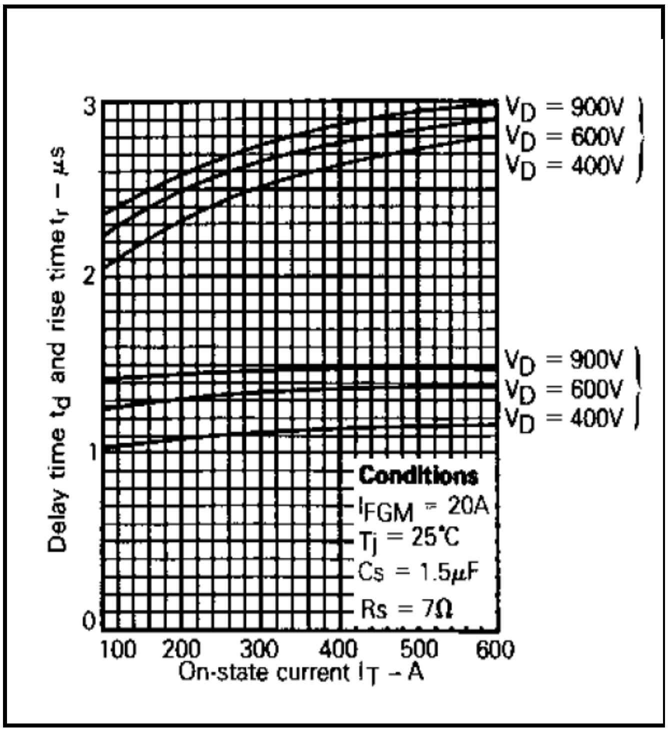
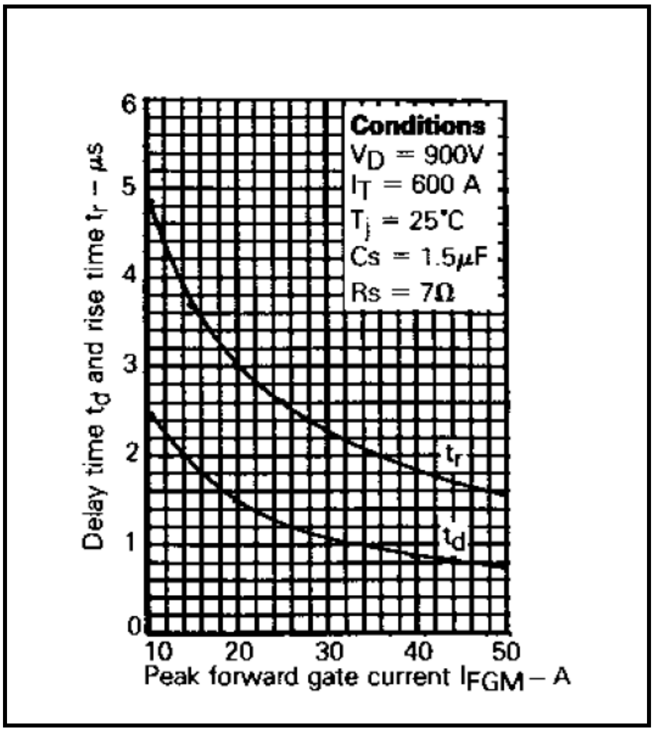


Fig.13 Turn-on energy vs rate of rise of on-state current

Fig.14 Delay time & rise time vs turn-on current



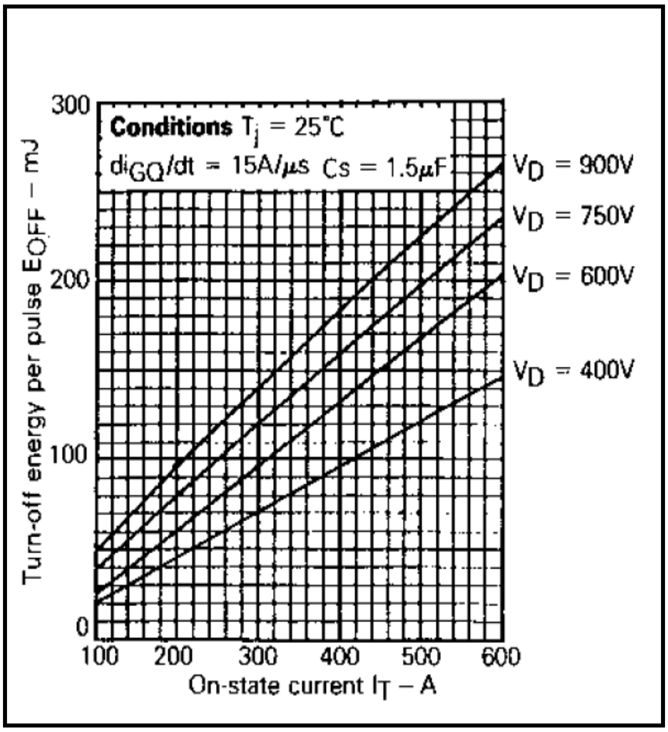


Fig.15 Delay time & rise time vs peak forward gate current

Fig.16 Turn-off energy vs on-state current

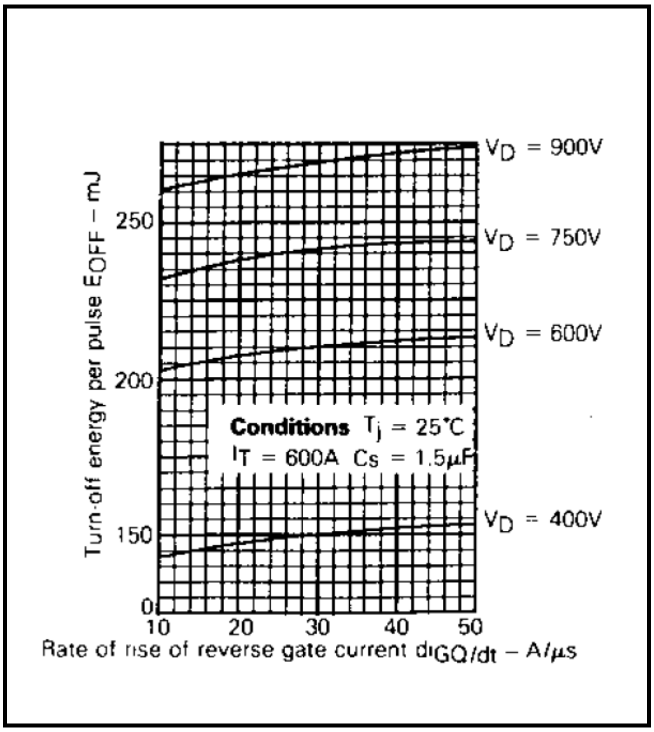


Fig.17 Turn-off energy vs rate of rise of reverse gate current

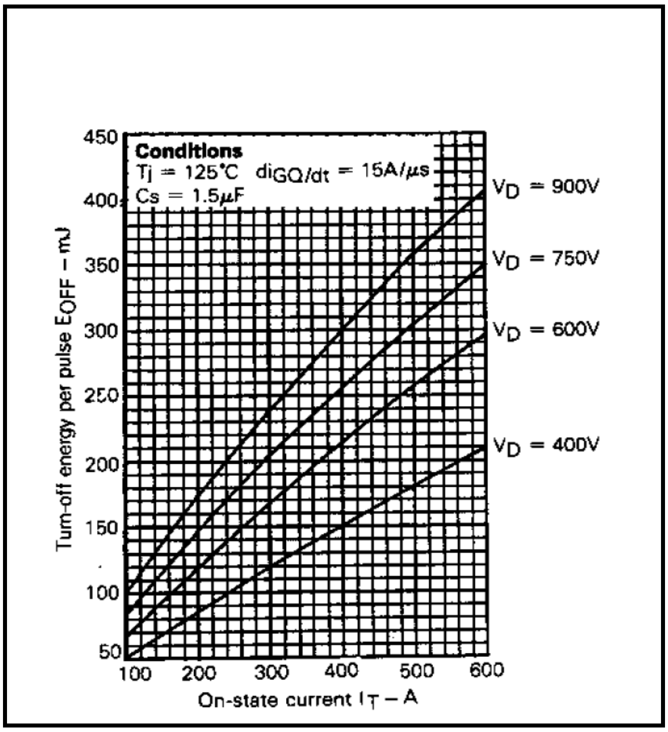


Fig.18 Turn-off energy vs on-state current

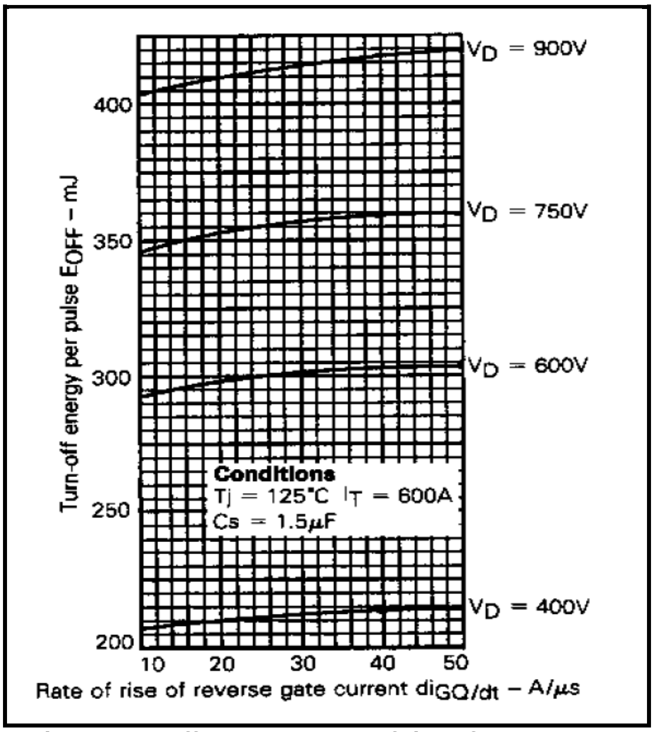


Fig.19 Turn-off energy vs rate of rise of reverse gate current

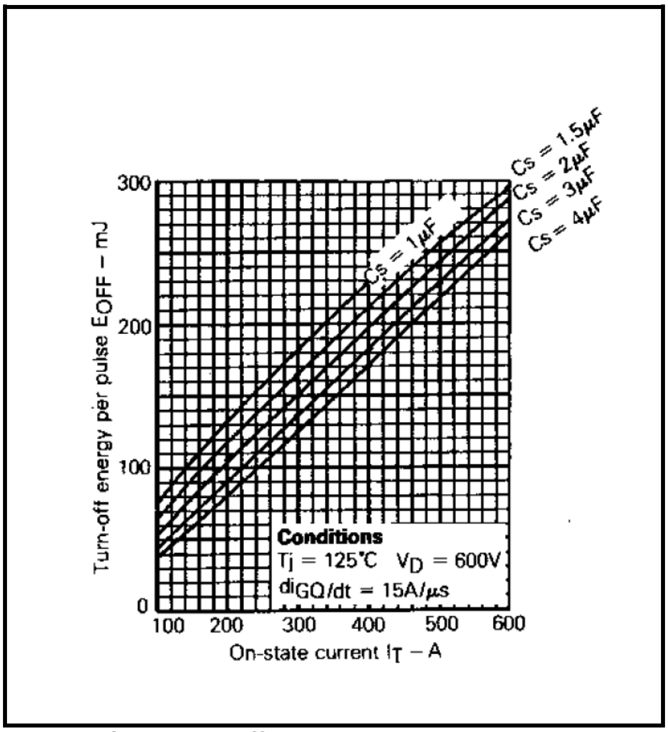


Fig.20 Turn-off energy vs on-state current

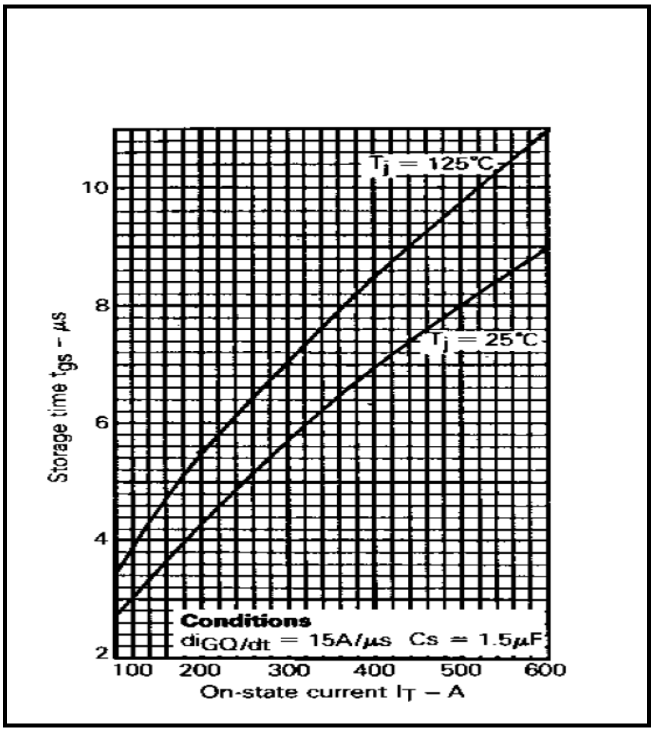


Fig.21 Gate storage time vs on-state current

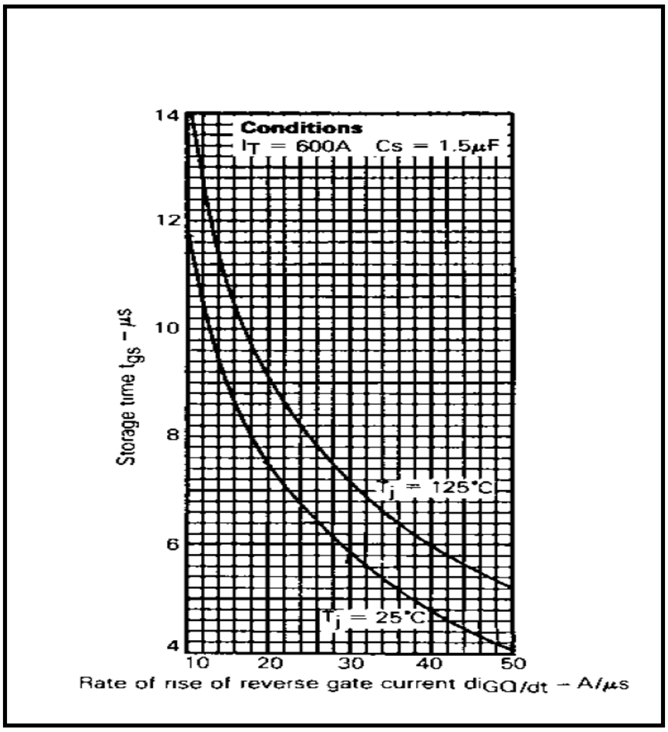


Fig.22 Gate storage time vs rate of rise of reverse gate current

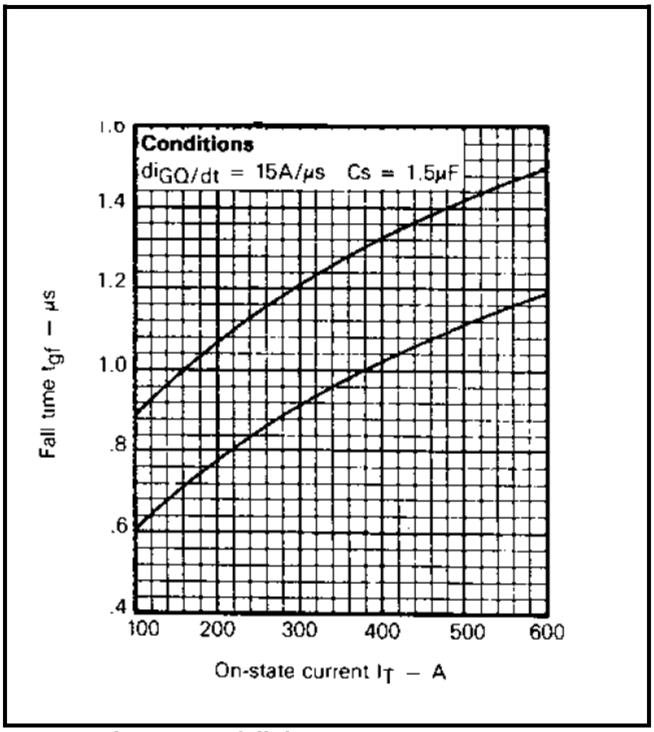


Fig.23 Gate fall time vs on-state current

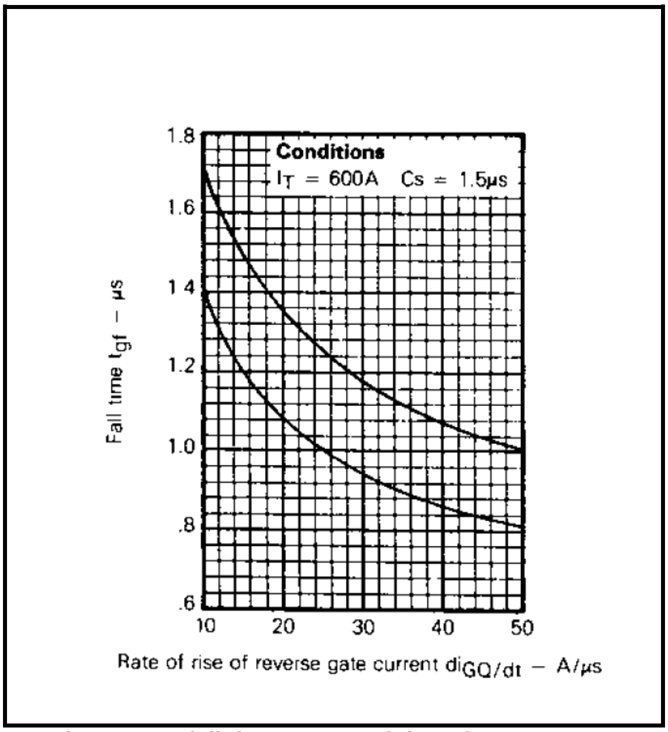


Fig.24 Gate fall time vs rate of rise of reverse gate current

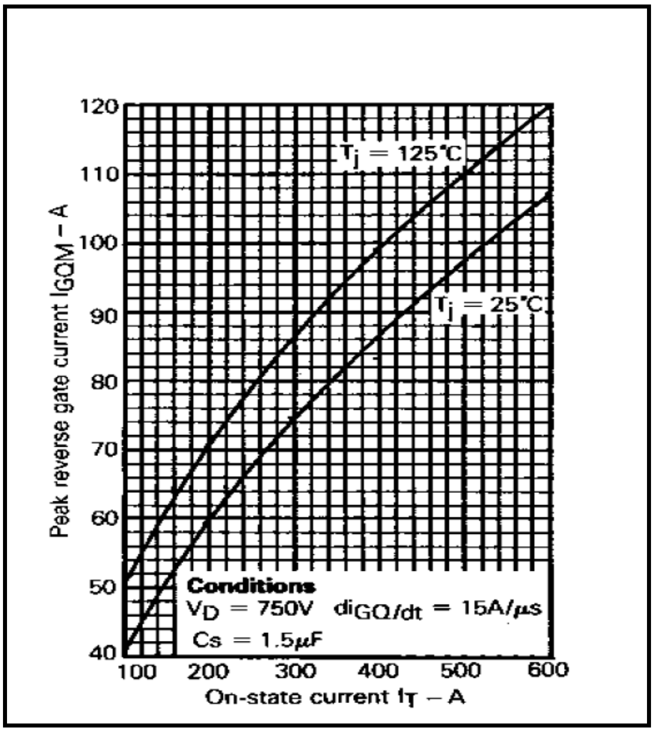


Fig.25 Peak reverse gate current vs turn-off current

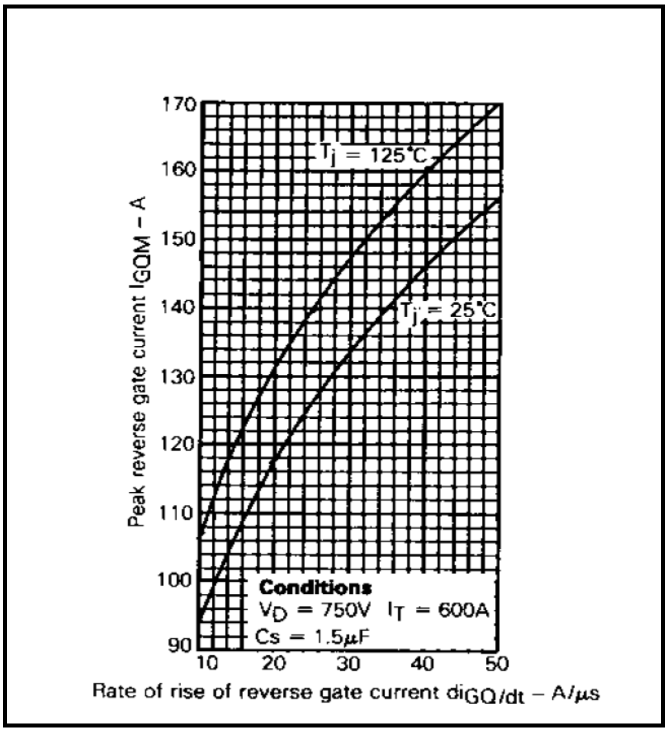


Fig.26 Peak reverse gate current vs rate of rise of reverse gate current

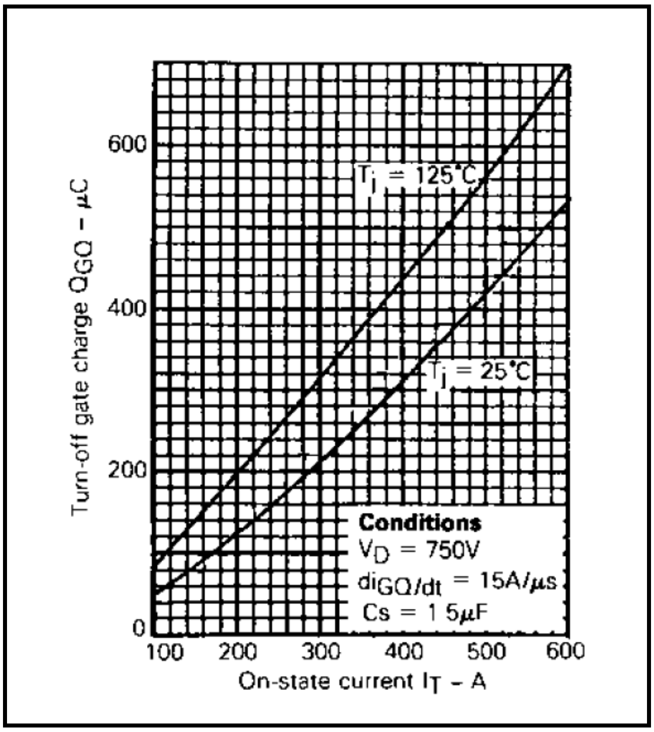


Fig.27 Turn-off gate charge vs on-state current

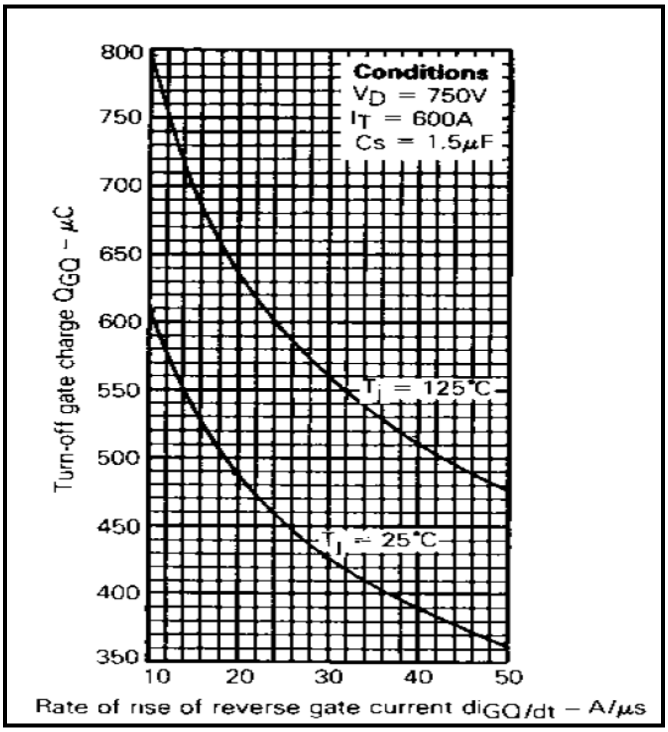


Fig.28 Turn-off gate charge vs rate of rise of reverse gate current

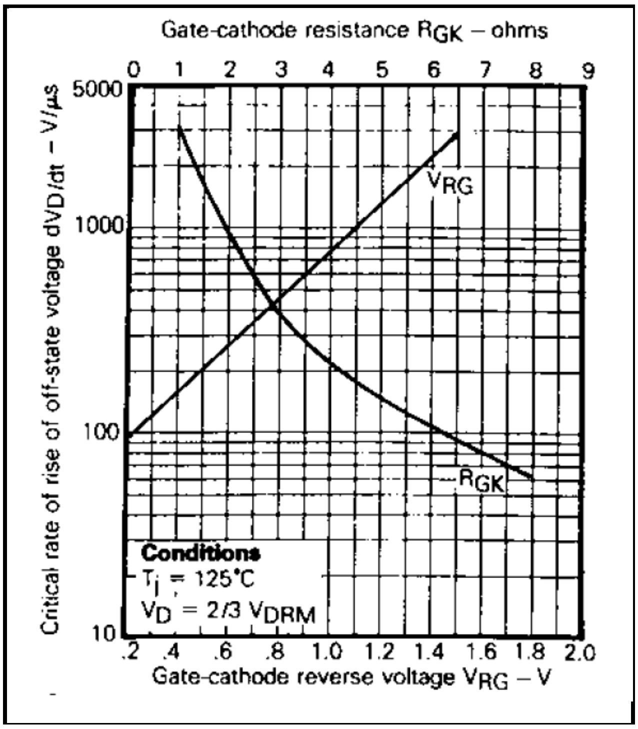
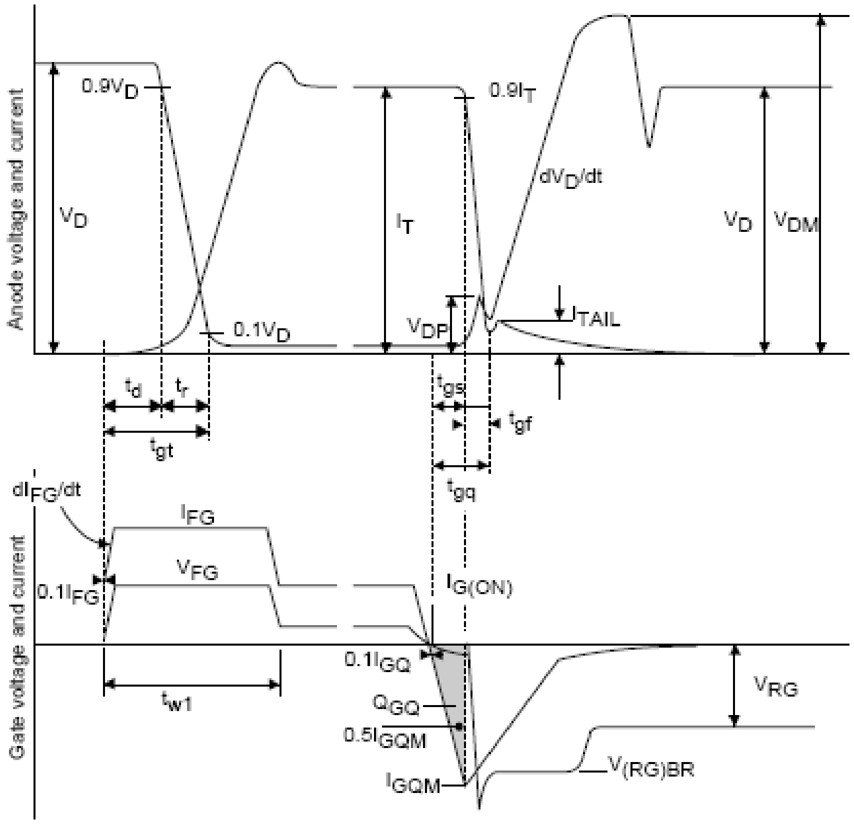


Fig.29 Dependence of critical dV_D/dt on gate-cathode Resistance and gate-cathode reverse voltage

Snubber Capacitor Cs (µF)	Snubber Resistor Rs (Ω)	Minimum Reset Time (µs)
2	7	35
	5	30
1.5	7	26
	5	22
1	7	17
	5	15

Table of snubber discharge time variation with snubber capacitor value.



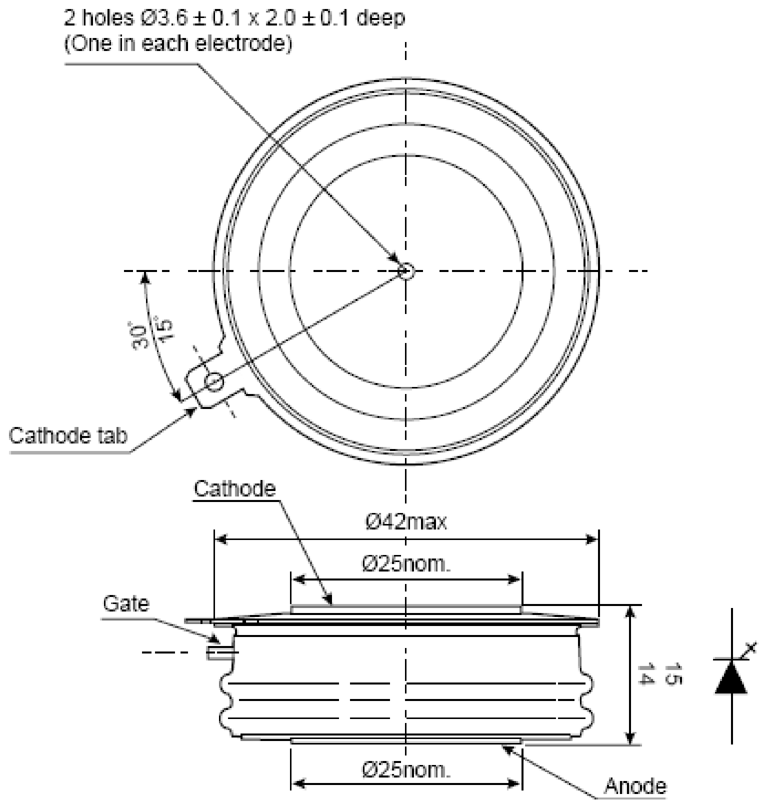
Recommended gate conditions:
I_{TCM} = 600A
I_{FG} = 20A
$I_{G(ON)}$ = 2A d.c.
$t_{w1(min)}$ = 10µs
I_{GQM} = 190A
di_{GQ}/dt = 15A/µs
Q_{GQ} = 1300µC
$V_{RG(min)}$ = 2.0V
$V_{RG(max)}$ = 16V

These are recommended Dynex Semiconductor conditions. Other conditions are permitted according to users gate drive specifications.

Fig.30 General switching waveforms

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise.
DO NOT SCALE.



Nominal weight: 82g
Clamping force: 6kN ±10%

Package outline type code: E

Fig.31 Package outline

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

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