

### FEATURES

- Double Side Cooling
- High Surge Capability

### APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

### KEY PARAMETERS

$V_{DRM}$	<b>4200V</b>
$I_{T(AV)}$	<b>780A</b>
$I_{TSM}$	<b>10500A</b>
$dV/dt^*$	<b>1500V/<math>\mu</math>s</b>
$dI/dt$	<b>400A/<math>\mu</math>s</b>

\*Higher  $dV/dt$  selections are available on request

### VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ (V)	Conditions
DCR780G42	4200	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 100\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR780G40	4000	
DCR780G38	3800	

Lower voltage grades available.

### ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR780G42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

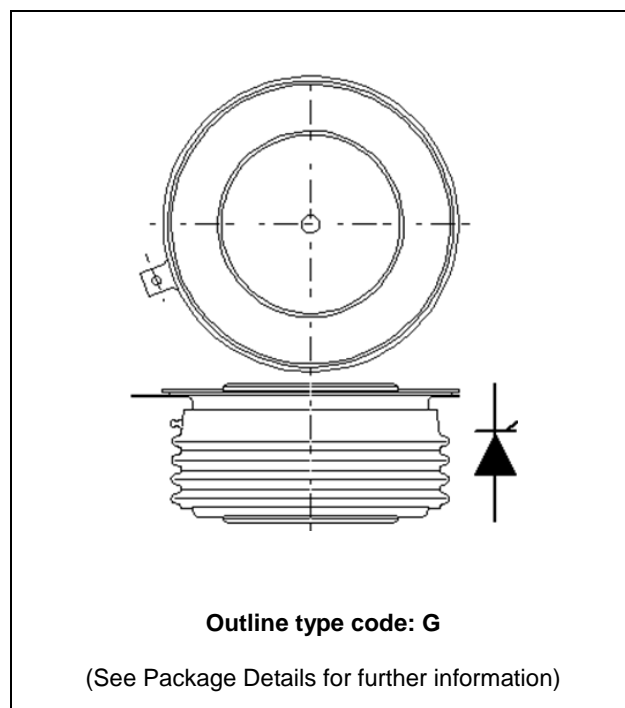


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	780	A
$I_{T(RMS)}$	RMS value	-	1230	A
$I_r$	Continuous (direct) on-state current	-	1170	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$ $V_R = 0$	10.5	kA
$I^2t$	$I^2t$ for fusing		0.55	MA <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	26.8	$^{\circ}\text{C/kW}$
		Single side cooled	Anode DC	-	52.7	$^{\circ}\text{C/kW}$
			Cathode DC	-	65.2	$^{\circ}\text{C/kW}$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 11.5kN (with mounting compound)	Double side	-	7.2	$^{\circ}\text{C/kW}$
			Single side	-	14.4	$^{\circ}\text{C/kW}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$		-	125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range			-55	125	$^{\circ}\text{C}$
$F_m$	Clamping force			10	13	kN

## DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
<b>I<sub>RRM</sub>/I<sub>DRM</sub></b>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	100	mA
<b>V<sub>TM</sub></b>	Instantaneous forward voltage	At 1600A peak, T <sub>j</sub> = 25°C		1.85	2.10	V
<b>dV/dt</b>	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C, gate open		-	1500	V/μs
<b>dI/dt</b>	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub> Gate source 30V, 10Ω tr < 0.5μs, T <sub>j</sub> = 125°C	Repetitive 50Hz	-	200	A/μs
			Non-repetitive	-	400	A/μs
<b>V<sub>T(TO)</sub></b>	Threshold voltage - Low level	100A to 500A at T <sub>case</sub> = 125°C		-	0.85	V
	Threshold voltage - High level	500A to 3000A at T <sub>case</sub> = 125°C		-	1.08	V
<b>r<sub>T</sub></b>	On-state slope resistance - Low level	100A to 500A at T <sub>case</sub> = 125°C		-	1.29	mΩ
	On-state slope resistance - High level	500A to 3000A at T <sub>case</sub> = 125°C		-	0.84	mΩ
<b>t<sub>gd</sub></b>	Delay time	V <sub>D</sub> = 67% V <sub>DRM</sub> , gate source 30V, 10Ω tr = 0.5μs, T <sub>j</sub> = 25°C		-	3	μs
<b>t<sub>q</sub></b>	Turn-off time	T <sub>j</sub> = 125°C, V <sub>R</sub> = 200V, dI/dt = 5A/μs, dV <sub>DR</sub> /dt = 20V/μs linear		300	600	μs
<b>Q<sub>s</sub></b>	Stored charge [LEM]	I <sub>T</sub> = 2000A, T <sub>j</sub> = 125°C, dI/dt = 5A/μs		1100	2200	μC
<b>Q<sub>s</sub></b>	Stored charge	T <sub>j</sub> = 125°C, dI/dt = 1A/μs, V <sub>R peak</sub> ~ 3400V, V <sub>R</sub> ~ 2600V		(Typ.) 1400		μC
<b>I<sub>RR</sub></b>	Reverse recovery current			(Typ.) 32		A
<b>I<sub>L</sub></b>	Latching current	T <sub>j</sub> = 25°C, V <sub>D</sub> = 5V		-	3	A
<b>I<sub>H</sub></b>	Holding current	T <sub>j</sub> = 25°C, R <sub>G-K</sub> = ∞, I <sub>TM</sub> = 500A, I <sub>T</sub> = 5A		-	300	mA

## GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	$V_{DRM} = 5V$ , $T_{case} = 25^{\circ}C$	1.5	V
$V_{GD}$	Gate non-trigger voltage	At 50% $V_{DRM}$ , $T_{case} = 125^{\circ}C$	0.4	V
$I_{GT}$	Gate trigger current	$V_{DRM} = 5V$ , $T_{case} = 25^{\circ}C$	350	mA
$I_{GD}$	Gate non-trigger current	At 50% $V_{DRM}$ , $T_{case} = 125^{\circ}C$	10	mA

## CURVES

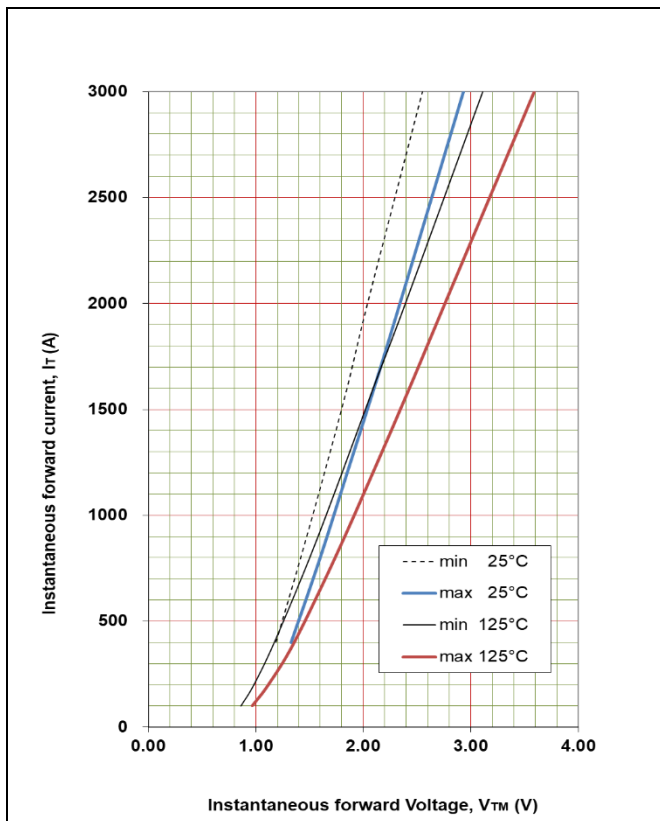


Fig. 2 Maximum & minimum on state characteristics

## $V_{TM}$ EQUATION

$$V_{TM} = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where  $A = 0.251538$

$B = 0.154177$

$C = 0.000839$

$D = -0.007547$

These values are valid for  $T_j = 125^{\circ}C$  for  $I_T$  100A to 3000A

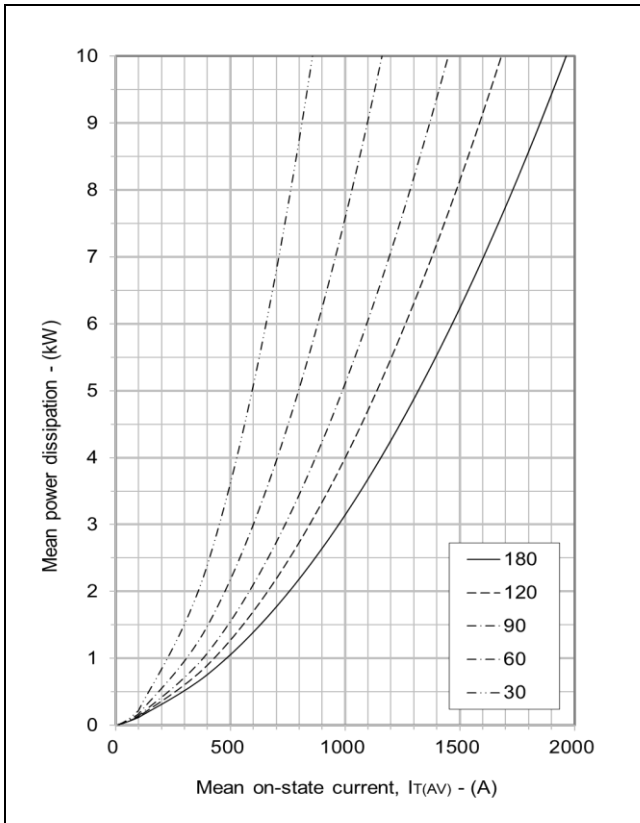


Fig. 3 On-state power dissipation - sine wave

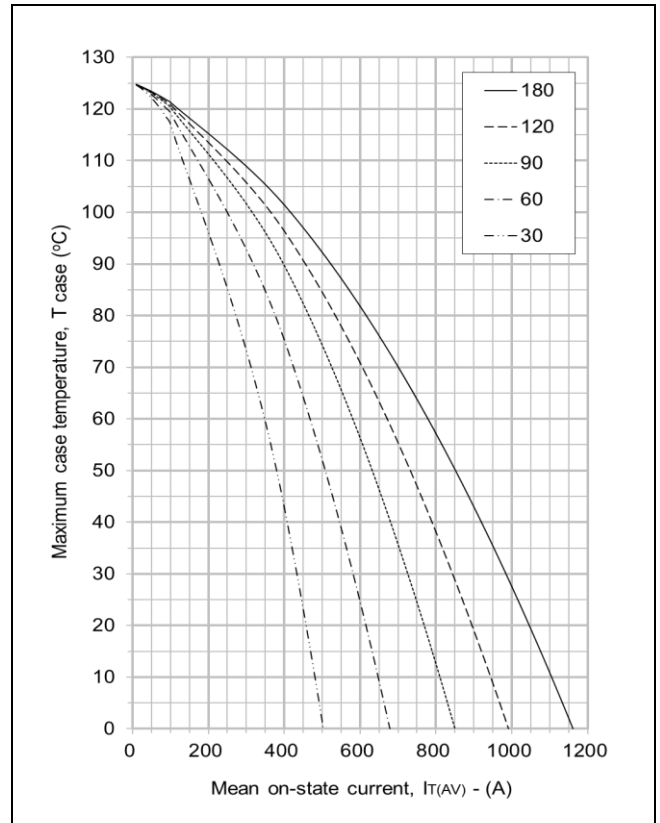


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

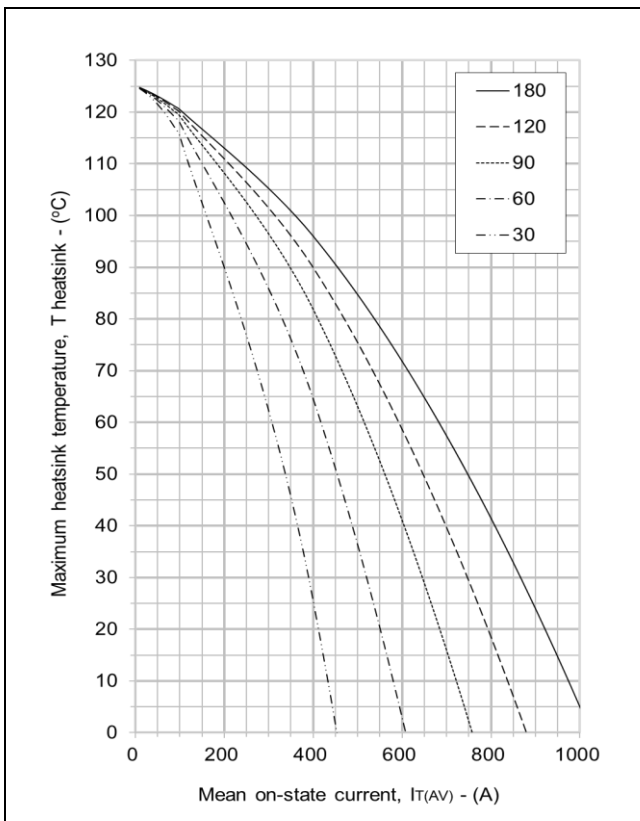


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

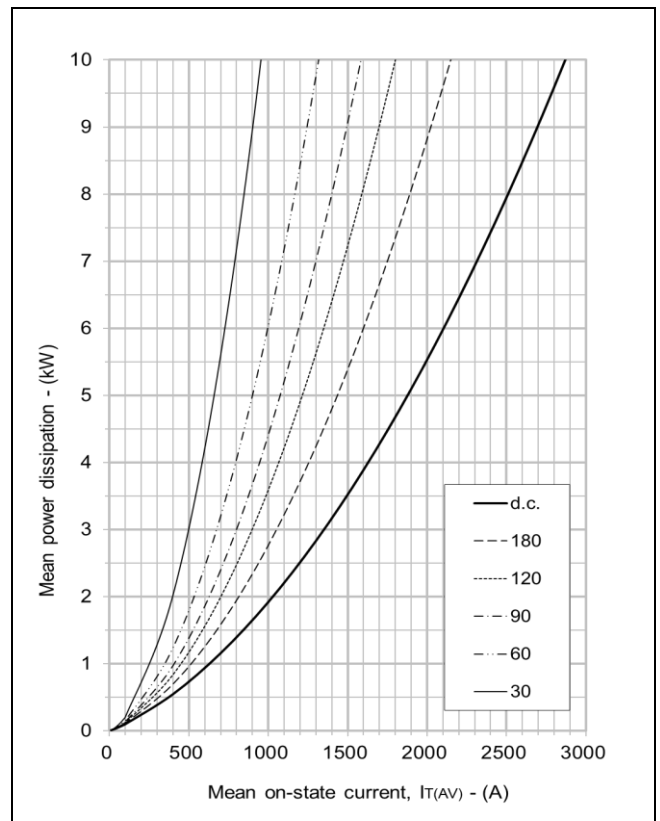


Fig. 6 On-state power dissipation - rectangular wave

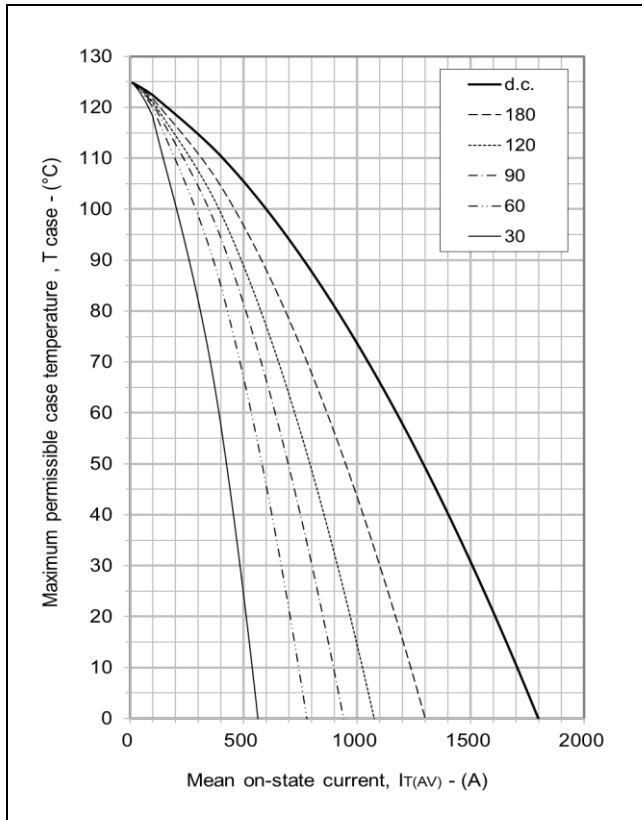


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

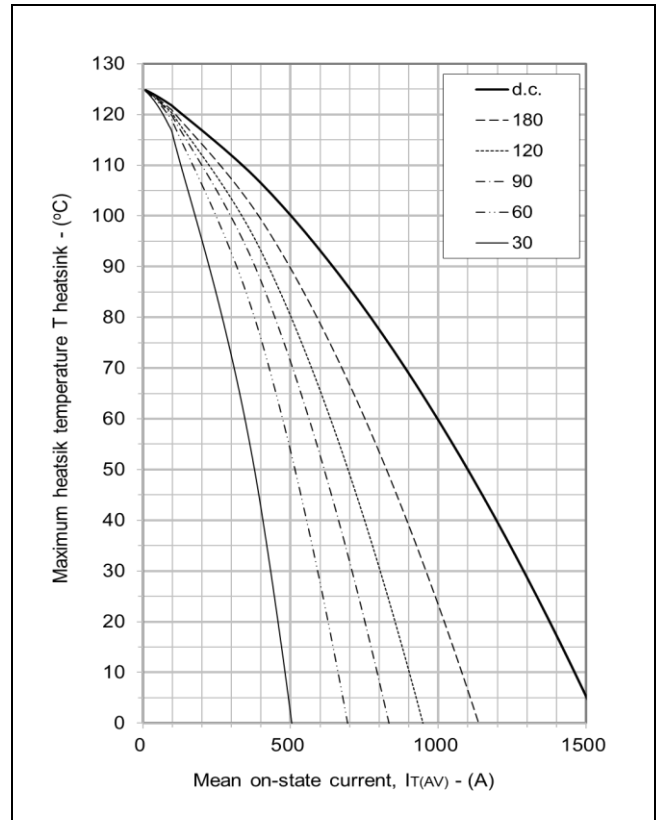


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

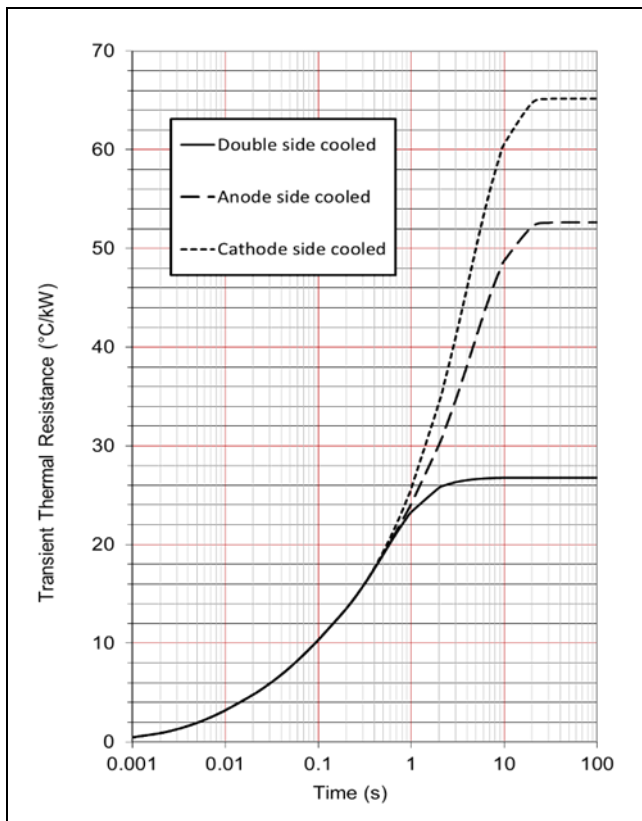


Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

		1	2	3	4
Double side cooled	Ri(°C/kW)	2.300	5.423	16.907	2.149
	Ti(s)	0.007	0.046	0.496	1.825
Anode side cooled	Ri(°C/kW)	2.321	5.266	10.269	34.803
	Ti(s)	0.007	0.046	0.348	4.582
Cathode side cooled	Ri(°C/kW)	2.490	5.911	7.426	49.343
	Ti(s)	0.007	0.053	0.393	4.230

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$  Conduction

Tables show the increments of thermal resistance  $R_{th(j-c)}$  when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
$\theta^*$	$\Delta Z_{th}(z)$		$\theta^*$	$\Delta Z_{th}(z)$		$\theta^*$	$\Delta Z_{th}(z)$	
	sine	rect		sine	rect		sine	rect
180	4.15	2.72	180	4.15	2.72	180	4.13	2.71
120	4.90	4.02	120	4.89	4.02	120	4.87	4.00
90	5.74	4.79	90	5.73	4.78	90	5.69	4.76
60	6.53	5.65	60	6.52	5.65	60	6.46	5.60
30	7.16	6.64	30	7.15	6.62	30	7.07	6.56
15	7.46	7.18	15	7.44	7.16	15	7.36	7.09

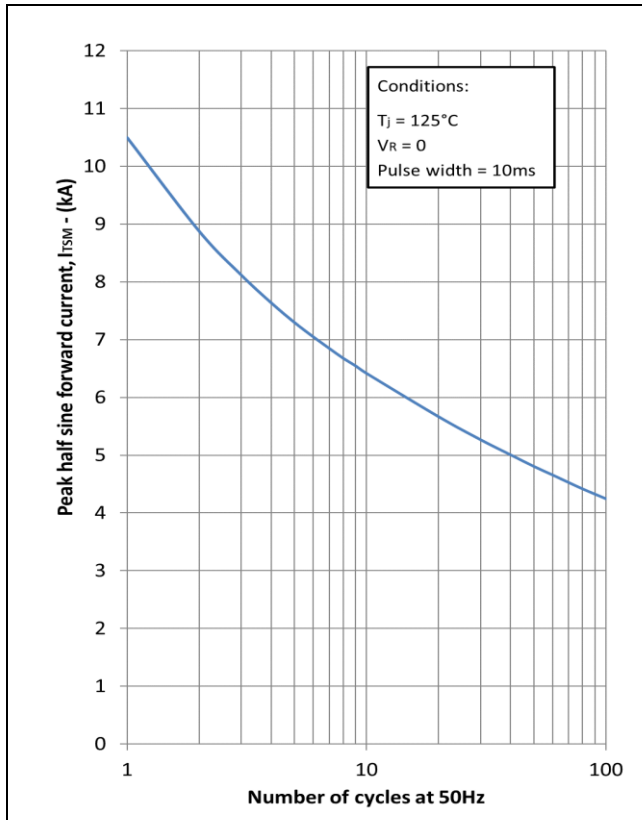


Fig. 10 Multi-cycle surge current

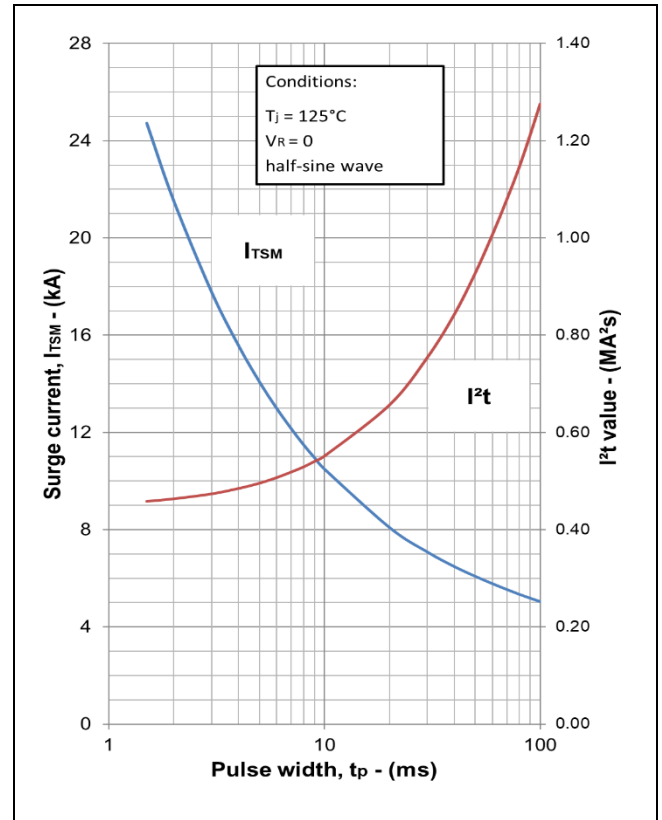


Fig. 11 Single-cycle surge current

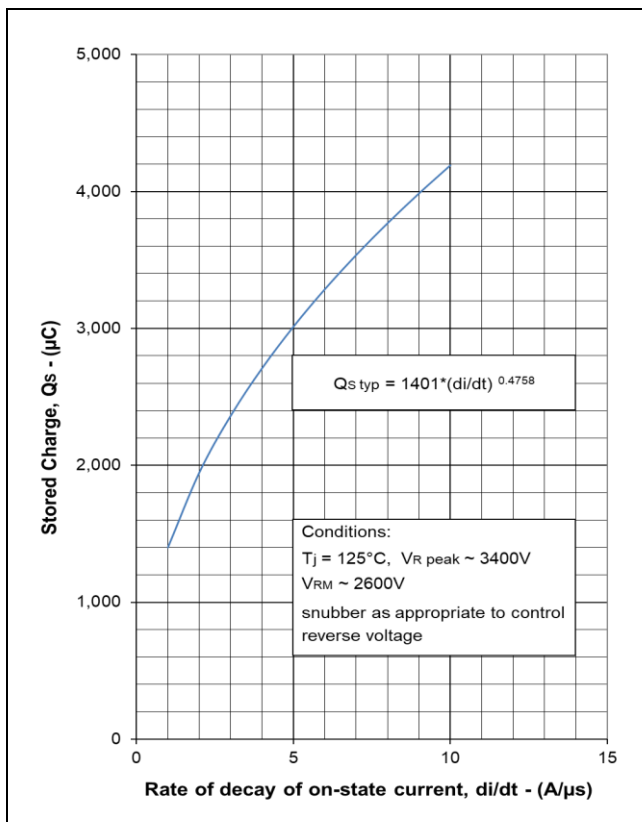


Fig. 12 Stored charge

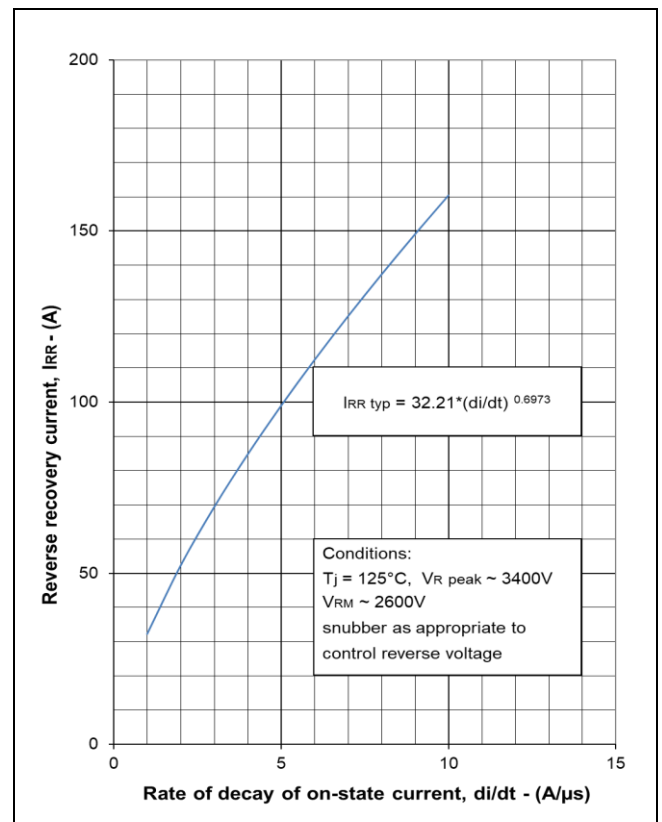


Fig. 13 Reverse recovery current

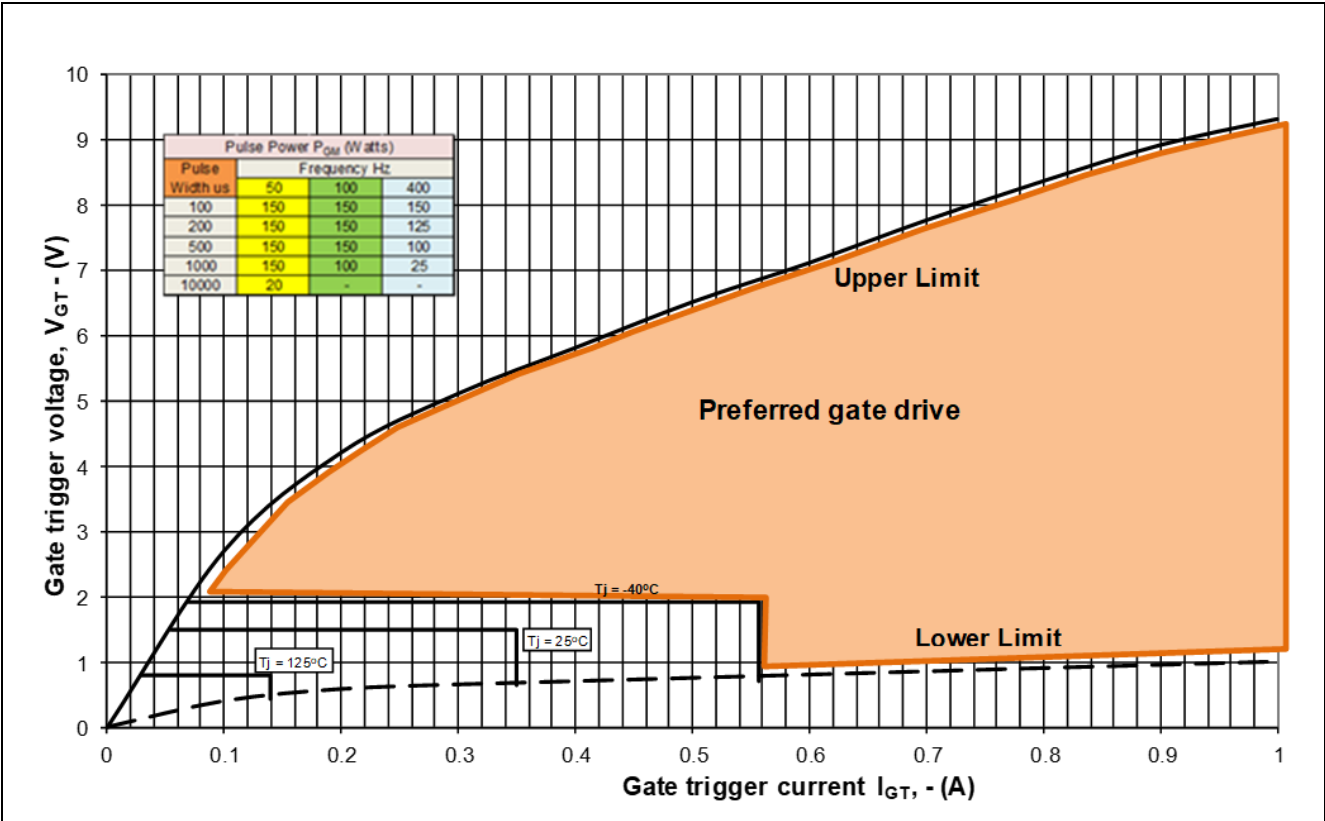


Fig. 14 Gate characteristics

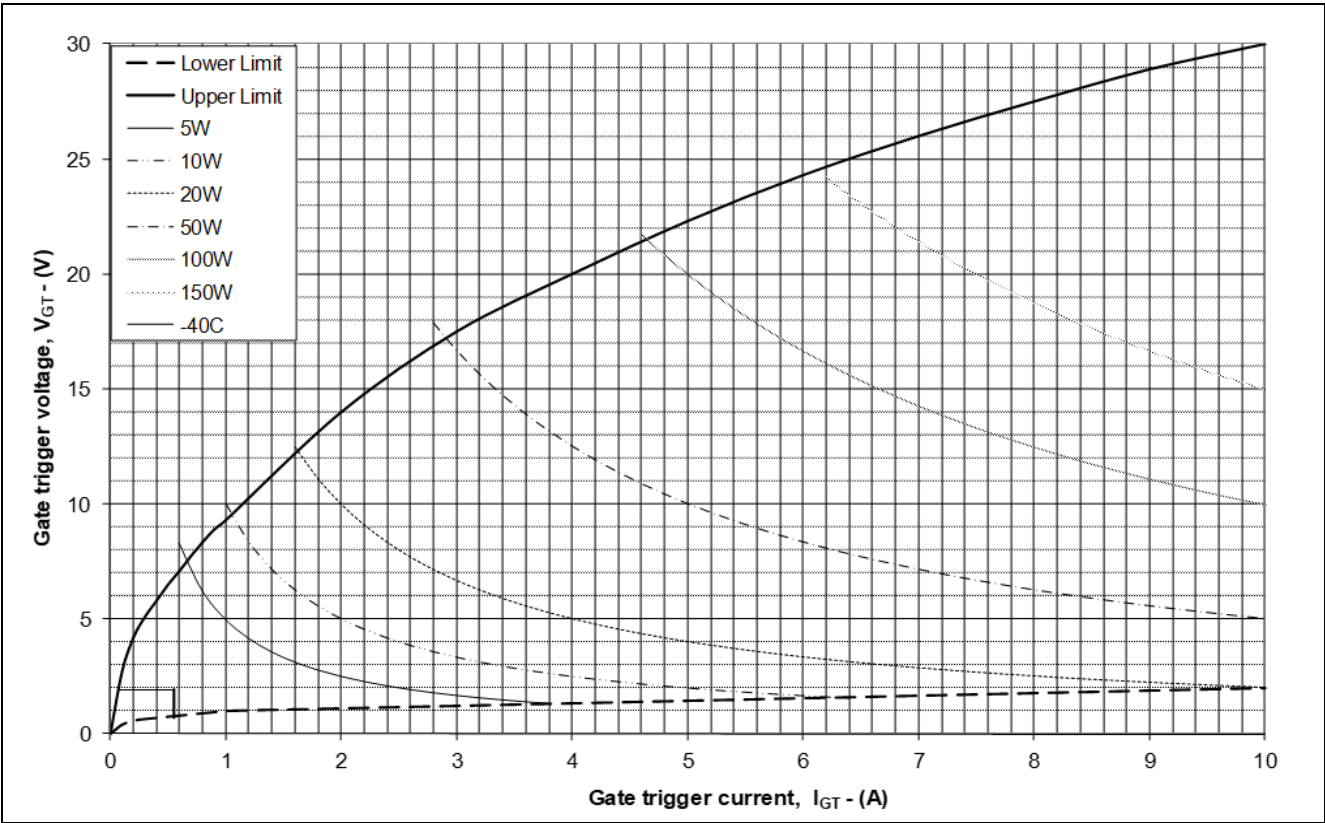


Fig. 15 Gate characteristics



## PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE

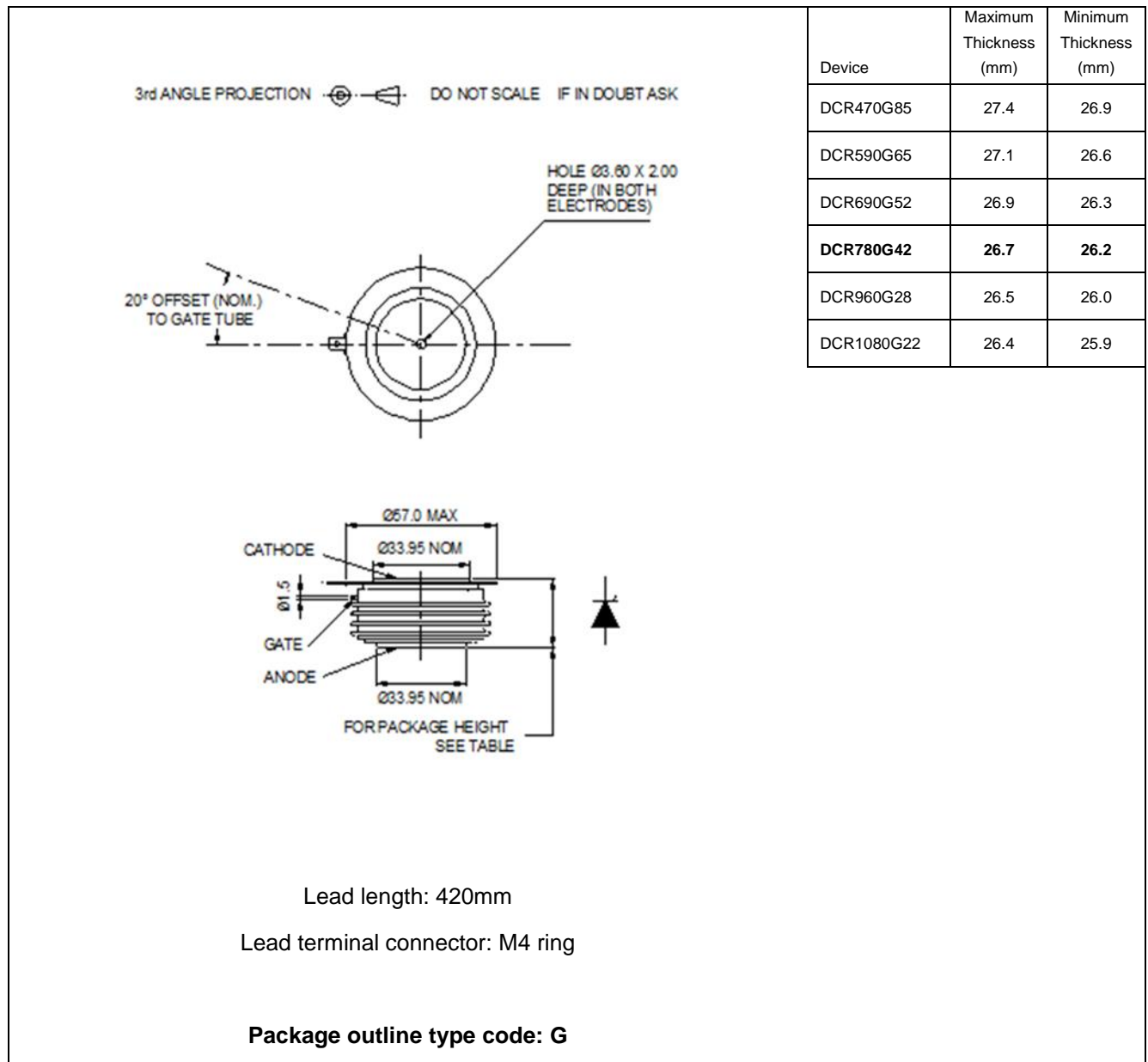


Fig. 16 Package outline

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