

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR5240H52*	5200	$T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 600\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR5240H50	5000	
DCR5240H48	4800	

Lower voltage grades available.
 *5000V @ -40°C , 5200V @ 0°C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR5240H52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	5200V
$I_{T(AV)}$	5240A
I_{TSM}	77800A
dV/dt^*	2000V/μs
di/dt	200A/μs

* Higher dV/dt selections available

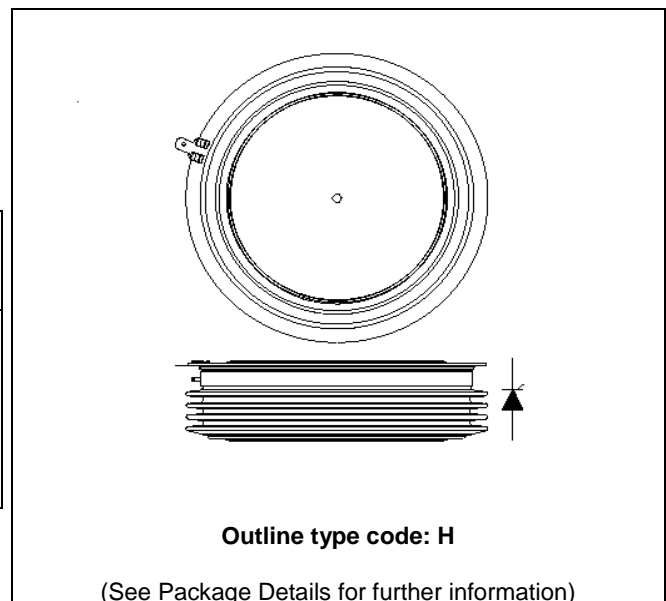


Fig. 1 Package outline

CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	5240	A
$I_{T(RMS)}$	RMS value	-	8230	A
I_T	Continuous (direct) on-state current	-	7290	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	77.80	kA
I^2t	I^2t for fusing	$V_R = 0$	30.27	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.004255	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.008	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0093	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 135.0kN (with mounting compound)	Double side	-	0.0009	$^{\circ}\text{C/W}$
			Single side	-	0.0018	$^{\circ}\text{C/W}$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}	-	125	$^{\circ}\text{C}$	
T_{stg}	Storage temperature range		-55	125	$^{\circ}\text{C}$	
F_m	Clamping force		120	155	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	600	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	2000	V/ μs
di/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$ Repetitive 50Hz	-	200	A/ μs
		Gate source 30V, 10 Ω , $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$ Non-repetitive	-	500	A/ μs
$V_{T(TO)}$	Threshold voltage – Low level	500 to 4000A at $T_{case} = 125^{\circ}C$	-	0.975	V
	Threshold voltage – High level	4000 to 8000A at $T_{case} = 125^{\circ}C$	-	1.222	V
r_T	On-state slope resistance – Low level	500A to 4000A at $T_{case} = 125^{\circ}C$	-	0.175	m Ω
	On-state slope resistance – High level	4000A to 8000A at $T_{case} = 125^{\circ}C$	-	0.118	m Ω
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu s$, $T_j = 25^{\circ}C$	-	3	μs
t_q	Turn-off time	$I_T = 3000A$, $T_j = 125^{\circ}C$, $V_R = 200V$, $di/dt = 1A/\mu s$, $dV_{DR}/dt = 20V/\mu s$ linear		500	μs
Q_S	Stored charge	$I_T = 3000A$, $T_j = 125^{\circ}C$, $di/dt = 1A/\mu s$, $V_{Rpeak} \sim 3100V$, $V_R \sim 2100V$	2230	4290	μC
I_{RR}	Reverse recovery current		38	52	A
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	-	3	A
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	0.4	V
I_{GT}	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	350	mA
I_{GD}	Gate non-trigger current	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	10	mA

CURVES

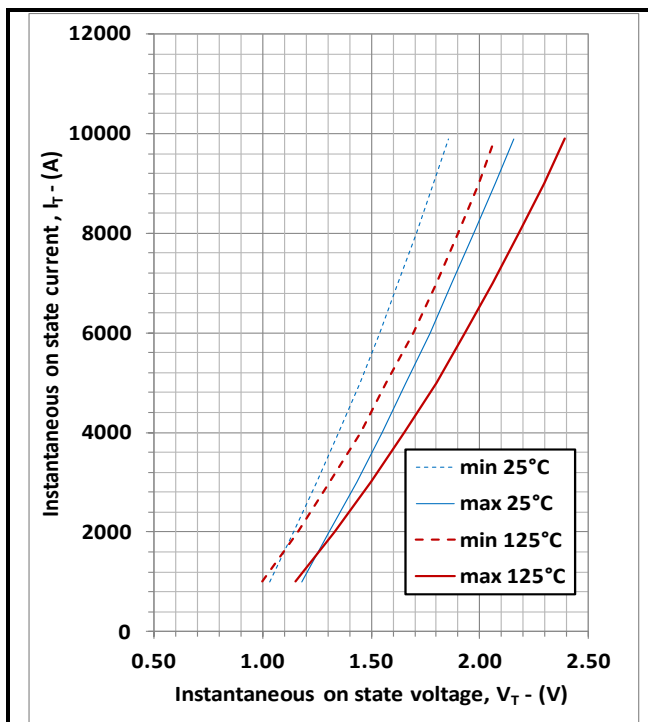


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where $A = 2.0022$
 $B = -0.2464$
 $C = -0.0000027$
 $D = 0.02699$

these values are valid for $T_j = 125^{\circ}C$ for I_T 500A to 8000A

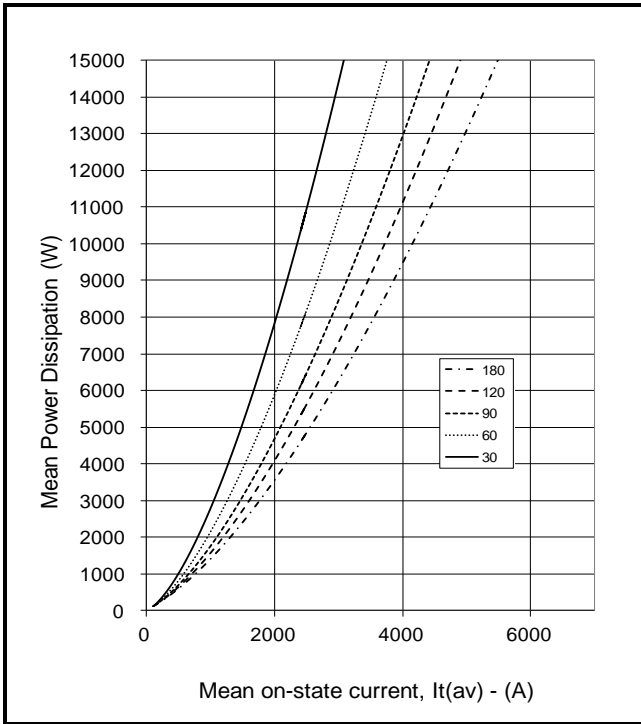


Fig.3 On-state power dissipation – sine wave

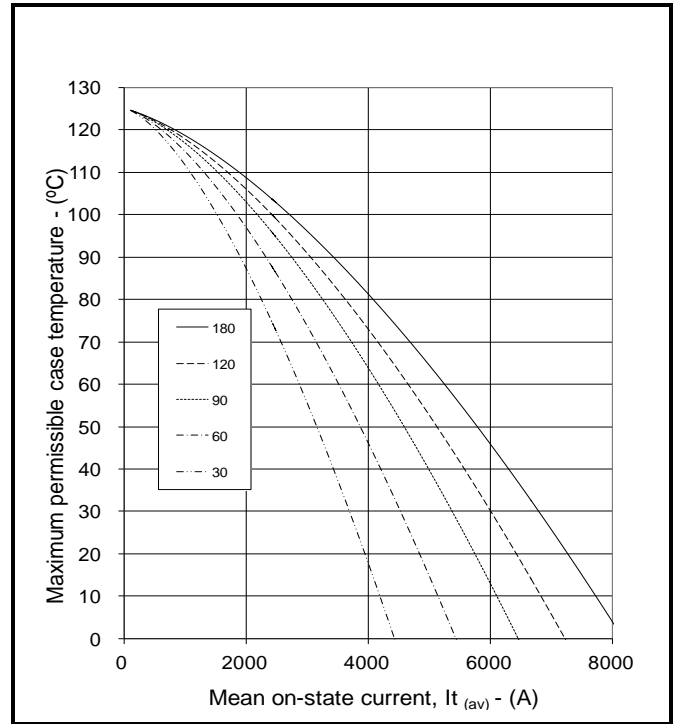


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

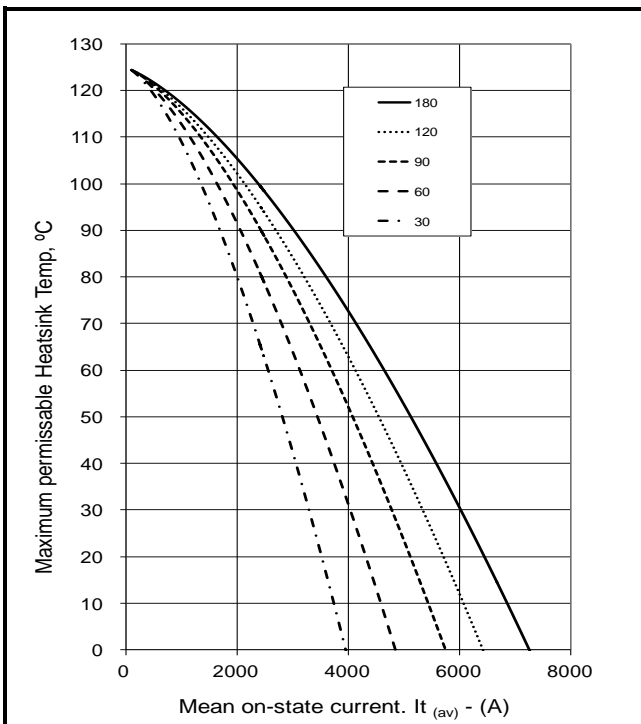


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

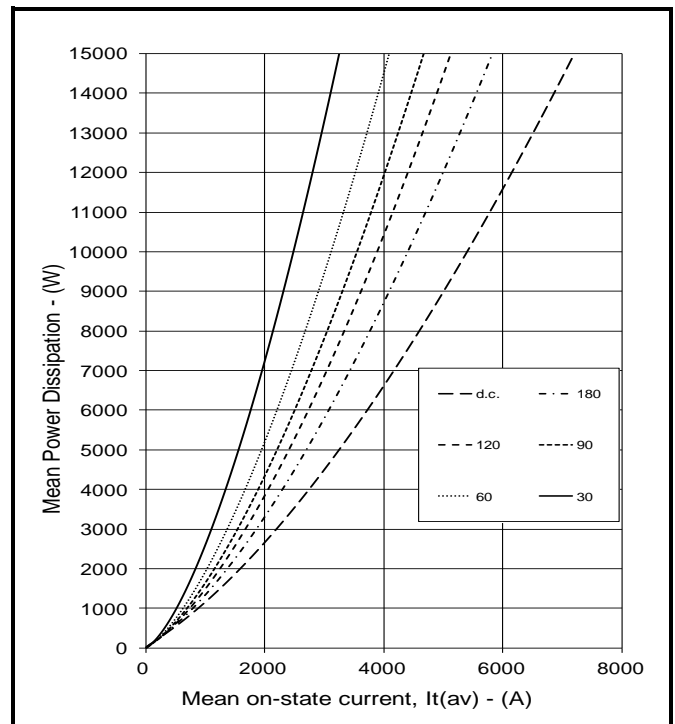


Fig.6 On-state power dissipation – rectangular wave

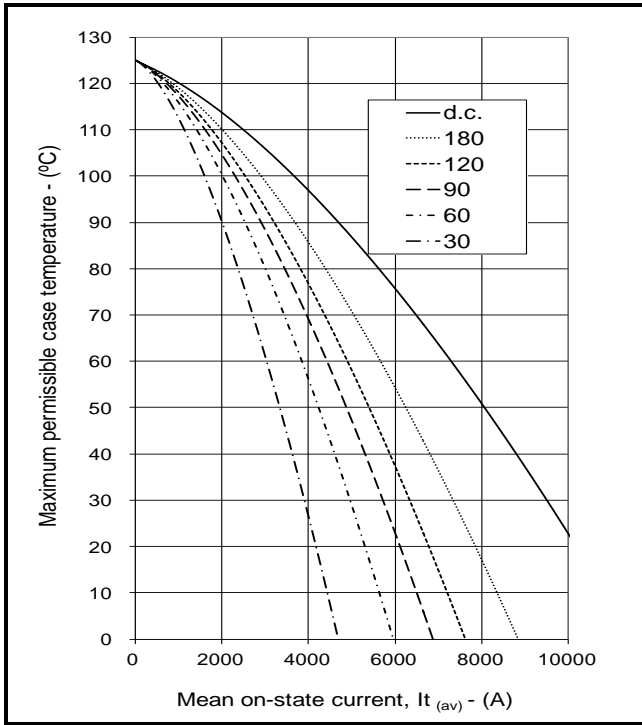


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

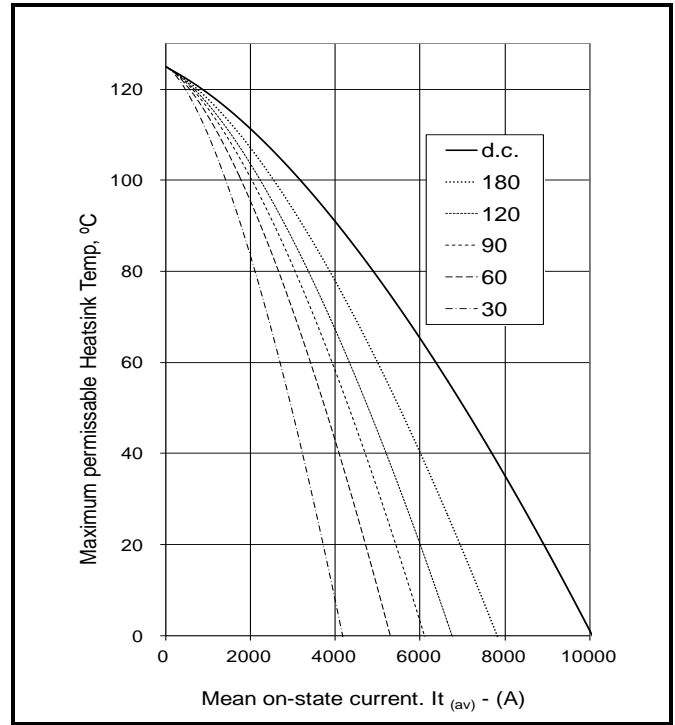


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

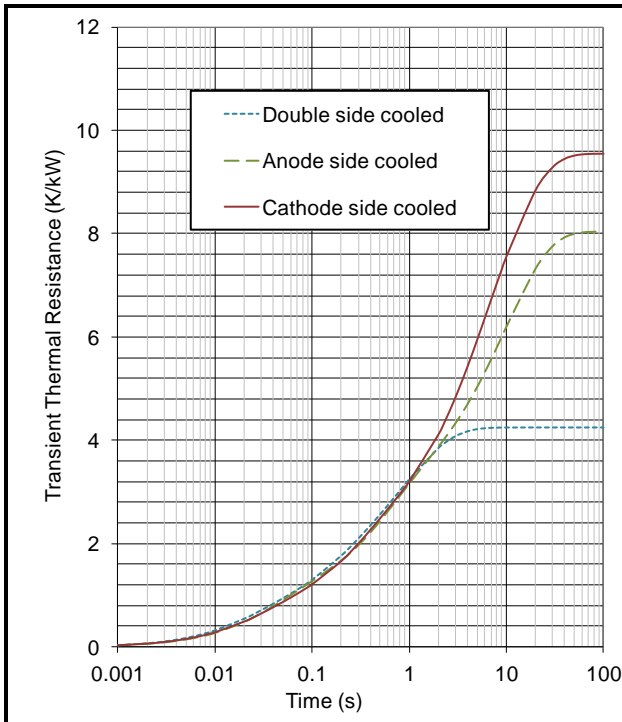


Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

		1	2	3	4
Double side cooled	R _i (°C/kW)	1.24786361	0.8334561	0.60621847	1.56769894
	T _i (s)	0.67007122	0.14563223	0.01981569	1.28702484
Anode side cooled	R _i (°C/kW)	0.51177271	1.94595762	0.91956601	4.66635596
	T _i (s)	2.89822124	0.50524092	0.0358286	10.6466908
Cathode side cooled	R _i (°C/kW)	2.41723953	1.53684913	0.62607497	4.9592331
	T _i (s)	3.44130269	0.26943359	0.02350127	10.172444

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(-T / T_i))]$$

ΔR_{th(j-c)} Conduction

Tables show the increments of thermal resistance R_{th(j-c)} when the device operates at conduction angles other than d.c.

θ°	Double side cooling		Anode Side Cooling		Cathode Sided Cooling	
	ΔZ _{th} (z)		ΔZ _{th} (z)		ΔZ _{th} (z)	
	sine.	rect.	sine.	rect.	sine.	rect.
180	0.38	0.26	0.32	0.23	0.33	0.23
120	0.44	0.37	0.36	0.31	0.38	0.33
90	0.49	0.43	0.41	0.36	0.43	0.37
60	0.54	0.49	0.45	0.40	0.47	0.43
30	0.58	0.55	0.48	0.45	0.51	0.48
15	0.60	0.58	0.49	0.48	0.52	0.51

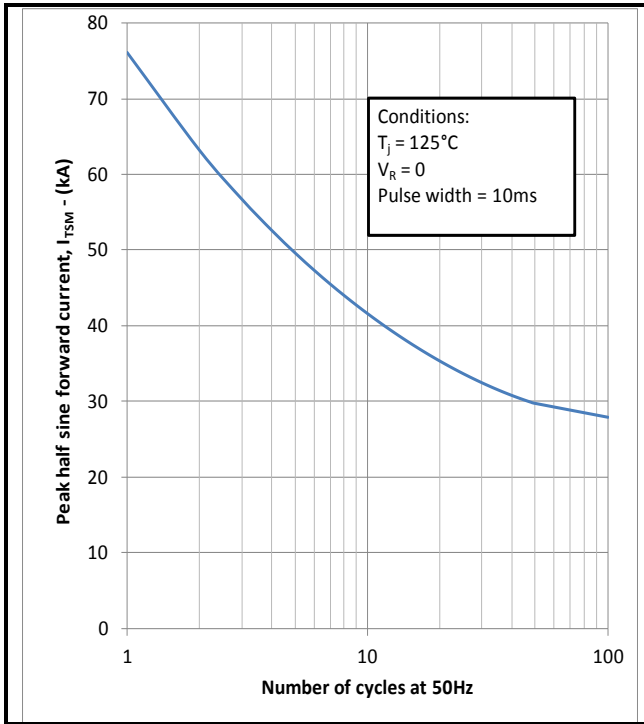


Fig.10 Multi-cycle surge current

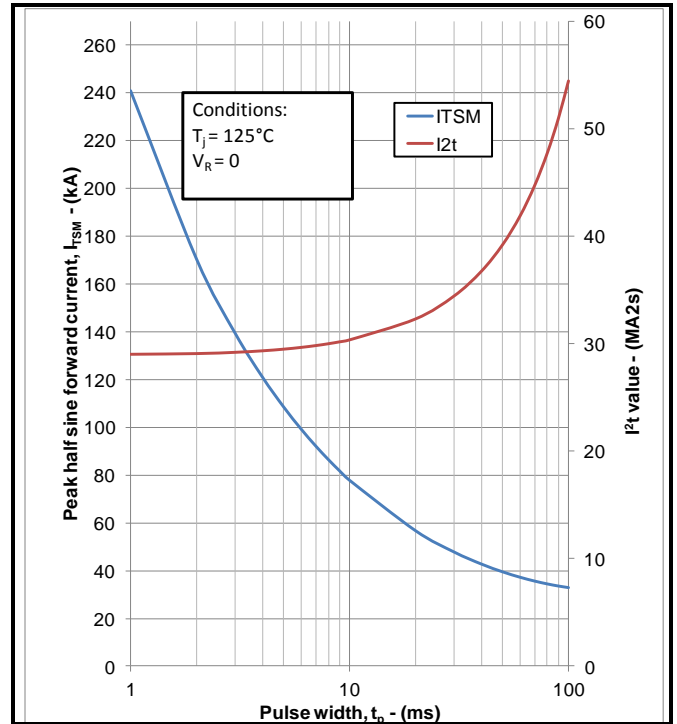


Fig.11 Single-cycle surge current

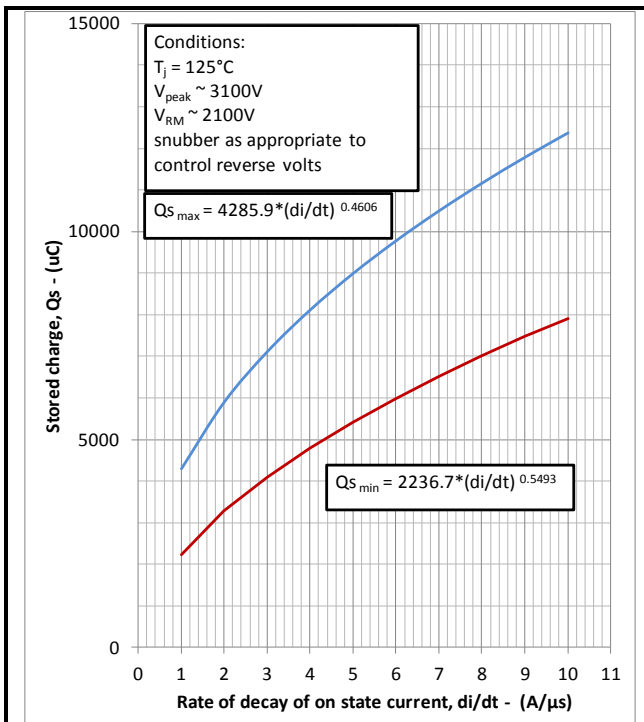


Fig.12 Stored charge

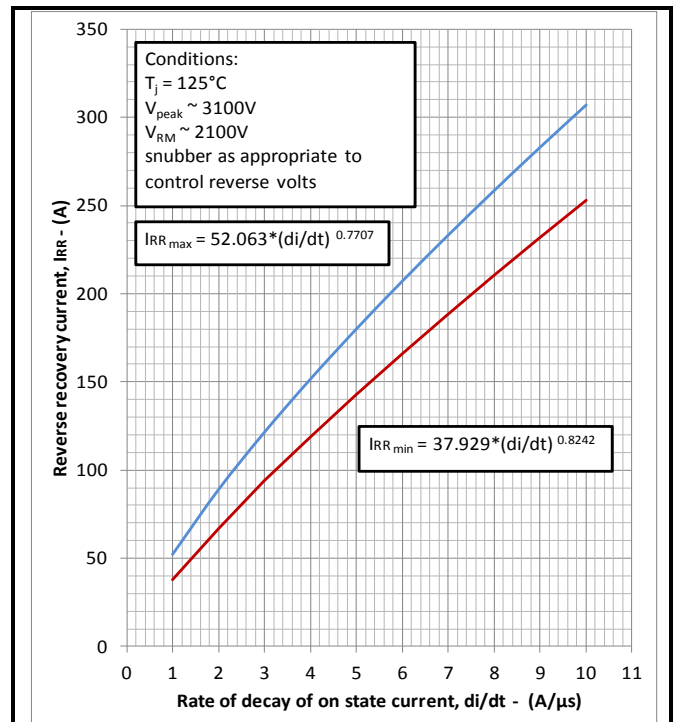


Fig.13 Reverse recovery current

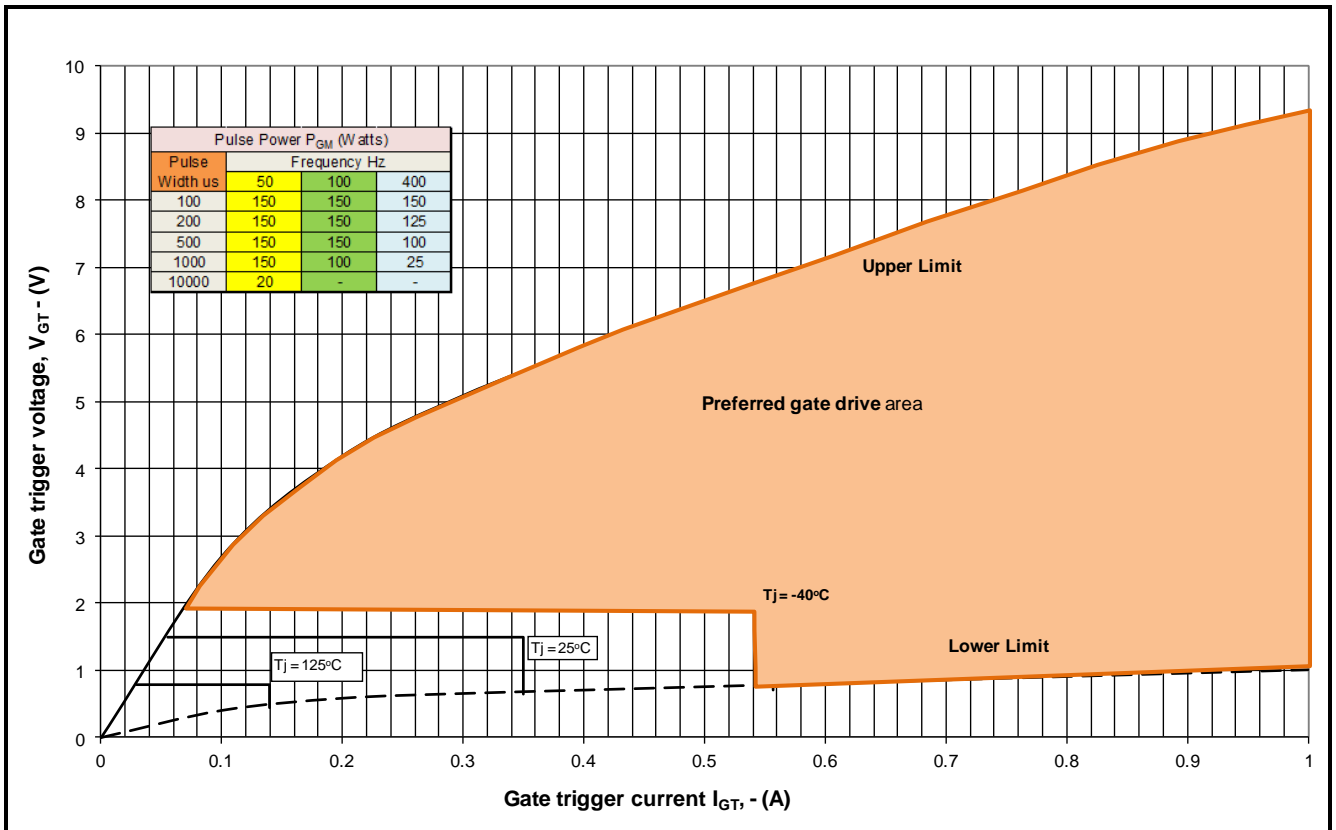


Fig14 Gate Characteristics

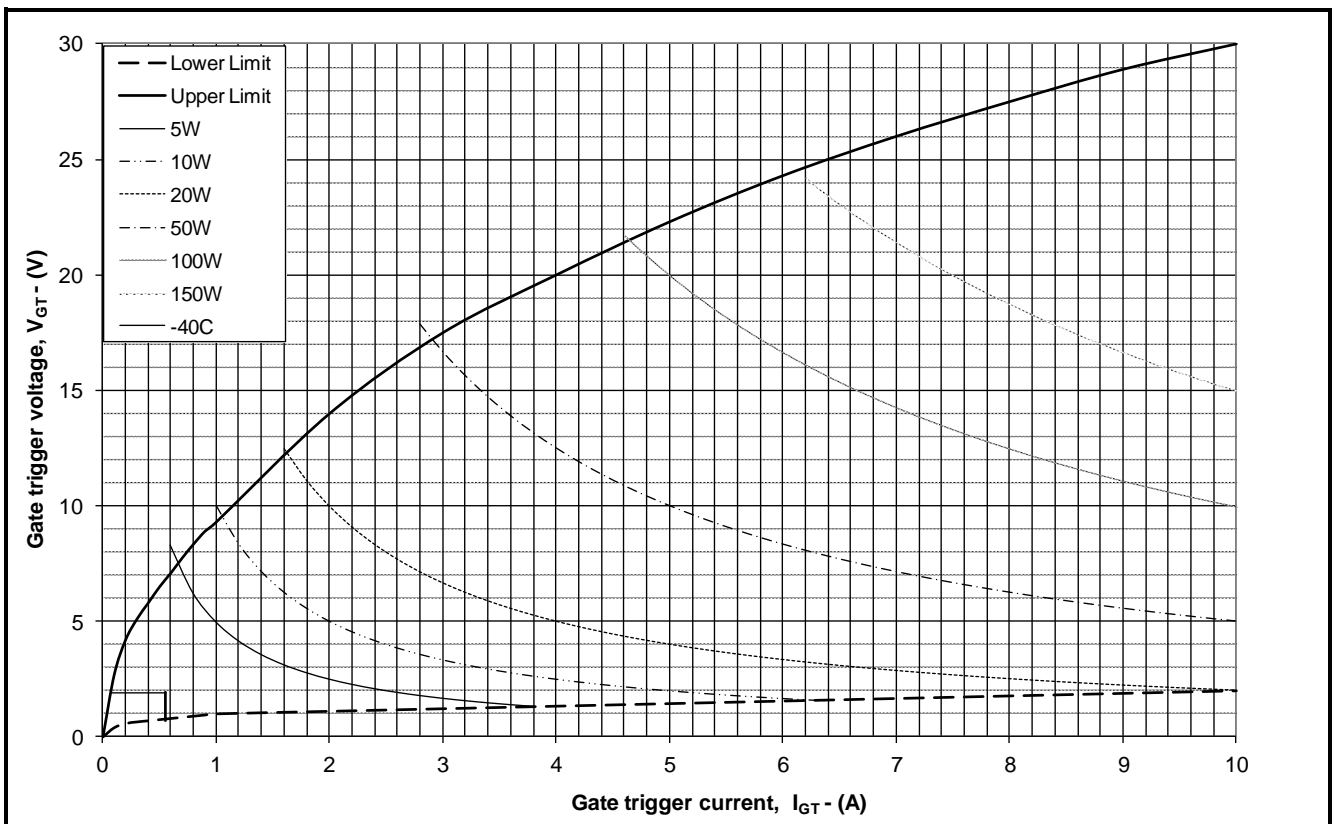
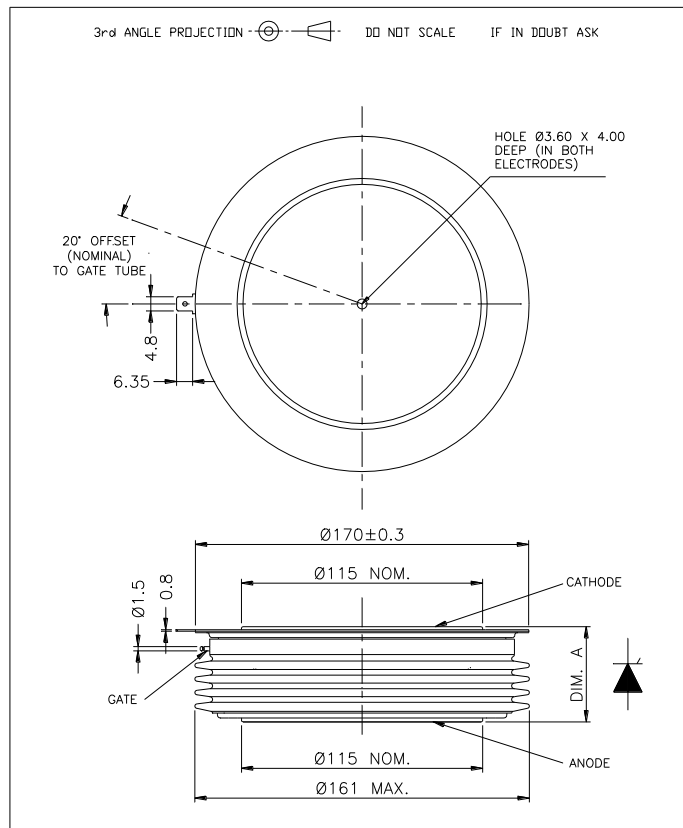


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR6140H42	35.15	34.28
DCR6650H42	35.15	34.28
DCR5240H52	35.27	34.4
DCR5890H52	35.27	34.4
DCR4420H65	35.3	34.7
DCR4660H65	35.3	34.7
DCR3640H85	35.65	35.05
DCR3980H85	35.65	35.05



Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code: H

Fig.16 Package outline

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The products must not be touched when operating because there is a danger of electrocution or severe burning. Always use protective safety equipment such as appropriate shields for the product and wear safety glasses. Even when disconnected any electric charge remaining in the product must be discharged and allowed to cool before safe handling using protective gloves.

Extended exposure to conditions outside the product ratings may affect reliability leading to premature product failure. Use outside the product ratings is likely to cause permanent damage to the product. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture, a large current to flow or high voltage arcing, resulting in fire or explosion. Appropriate application design and safety precautions should always be followed to protect persons and property.

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Preliminary Information:	The product design is complete and final characterisation for volume production is in progress. The datasheet represents the product as it is now understood but details may change.
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