DCR490J65

Phase Control Thyristor

Replaces DS5832-3

DS5832-4 December 2024 (LN43772)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

V_{DRM}	**6500V**
$I_{T(AV)}$	**490A**
I_{TSM}	**6600A**
dV/dt*	**1500V/µs**
dI/dt	**200A/µs**

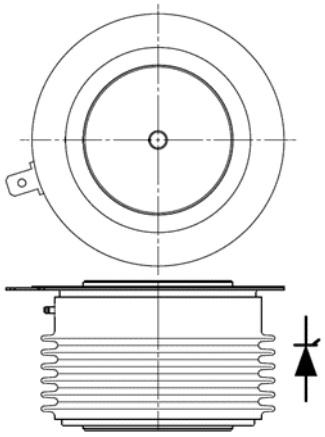
***Higher dV/dt selections are available on request**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
DCR490J65* DCR490J60 DCR490J55	6500 6000 5500	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 100mA, V_{DRM}, V_{RRM} t_p = 10ms V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

*6200V @ -40°C, 6500V @ 0°C



Outline type code: J

(See Package Details for further information)

Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR490J65

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	490	A
$I_{T(RMS)}$	RMS value	-	770	A
I_T	Continuous (direct) on-state current	-	730	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C V_R = 0	6.60	kA
I^2t	I^2t for fusing		0.22	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	37.8	°C/kW
		Single side cooled	Anode DC	-	74.3	°C/kW
			Cathode DC	-	79.5	°C/kW
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 11.5kN (with mounting compound)	Double side	-	7.2	°C/kW
			Single side	-	14.4	°C/kW
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			10	13	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	100	mA
V_{TM}	Instantaneous forward voltage	At 1600A peak, T_j = 25°C		2.60	3.00	V
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$ Gate source 30V, 10Ω t_r < 0.5µs, T_j = 125°C	Repetitive 50Hz	-	100	A/µs
			Non-repetitive	-	200	A/µs
$V_{T(TO)}$	Threshold voltage - Low level	100A to 400A at T_{case} = 125°C		-	0.93	V
	Threshold voltage - High level	400A to 1600A at T_{case} = 125°C		-	1.12	V
r_T	On-state slope resistance - Low level	100A to 400A at T_{case} = 125°C		-	2.10	mΩ
	On-state slope resistance - High level	400A to 1600A at T_{case} = 125°C		-	1.65	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	I_T = 500A, T_j = 125°C, V_R = 100V, dI/dt = 5A/µs, dV_{DR}/dt = 20V/µs linear		550	1100	µs
Q_S	Stored charge	I_T = 500A, T_j = 125°C, dI/dt = 5A/µs [LEM]		1800	2600	µC
I_{RR}	Reverse recovery current			77	90	A
Q_S	Stored charge	T_j = 125°C, dI/dt = 1A/µs, $V_{R\ peak}$ ~ 3900V, V_R ~ 2450V		1570	2570	µC
I_{RR}	Reverse recovery current			32	38	A
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	350	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	15	mA

CURVES

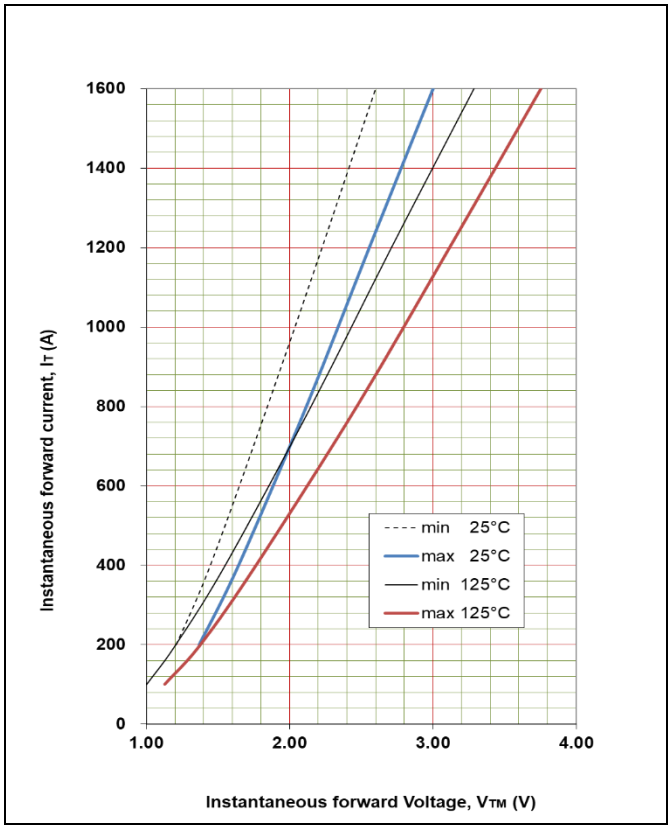


Fig. 2 Maximum & minimum on state characteristics

V_{TM} EQUATION

$V_{TM} = A + B.\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.330904
B = 0.141361
C = 0.001495
D = -0.000337

These values are valid for T_j = 125°C for I_T 100A to 1600A

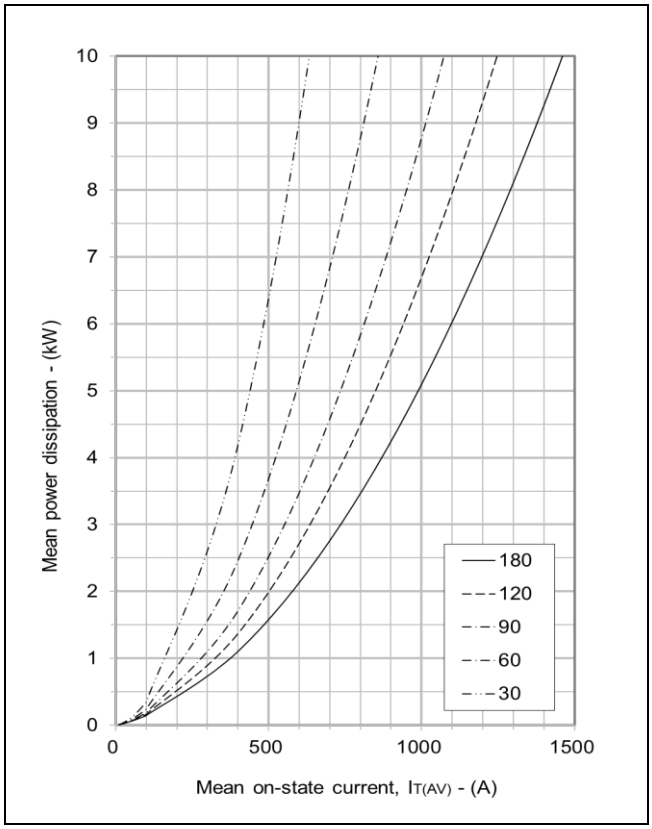


Fig. 3 On-state power dissipation - sine wave

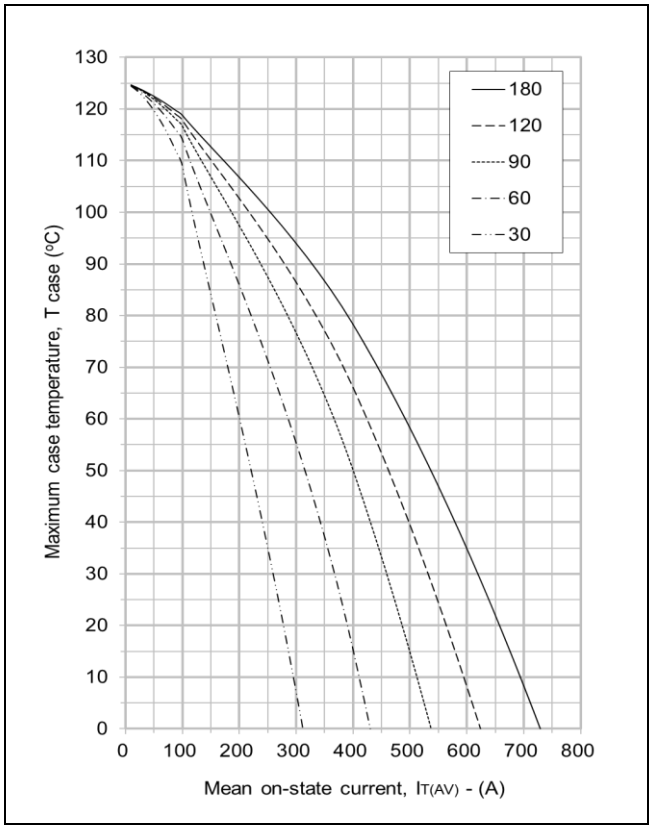


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

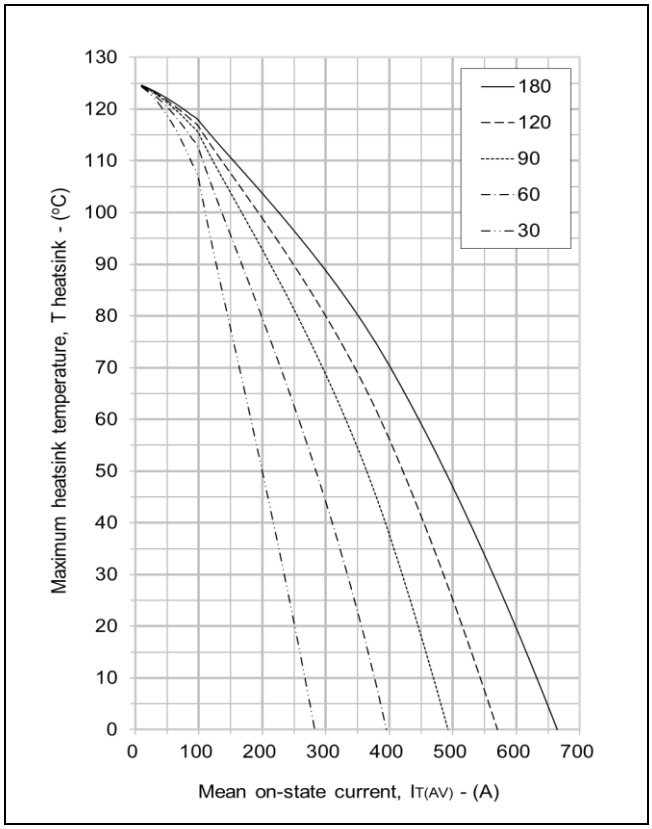


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

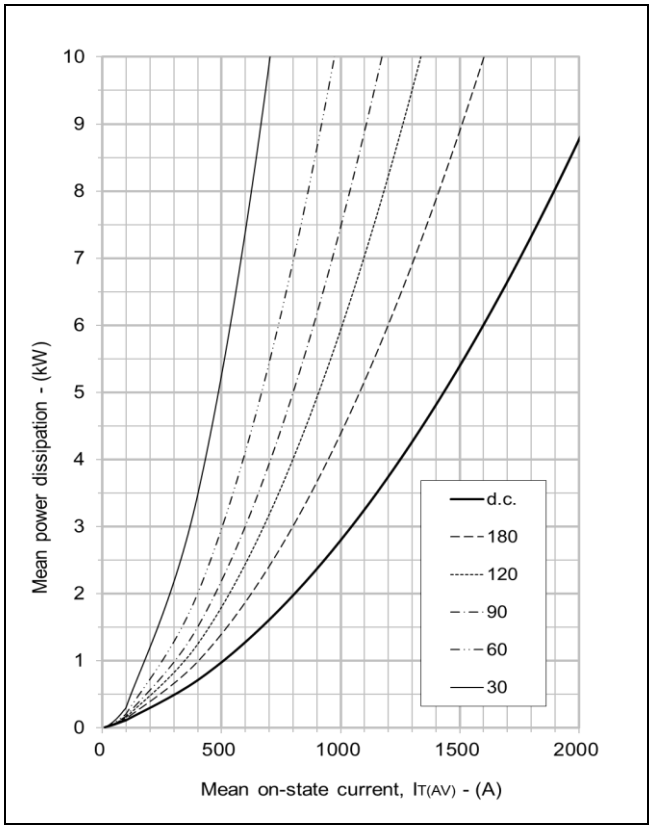


Fig. 6 On-state power dissipation - rectangular wave

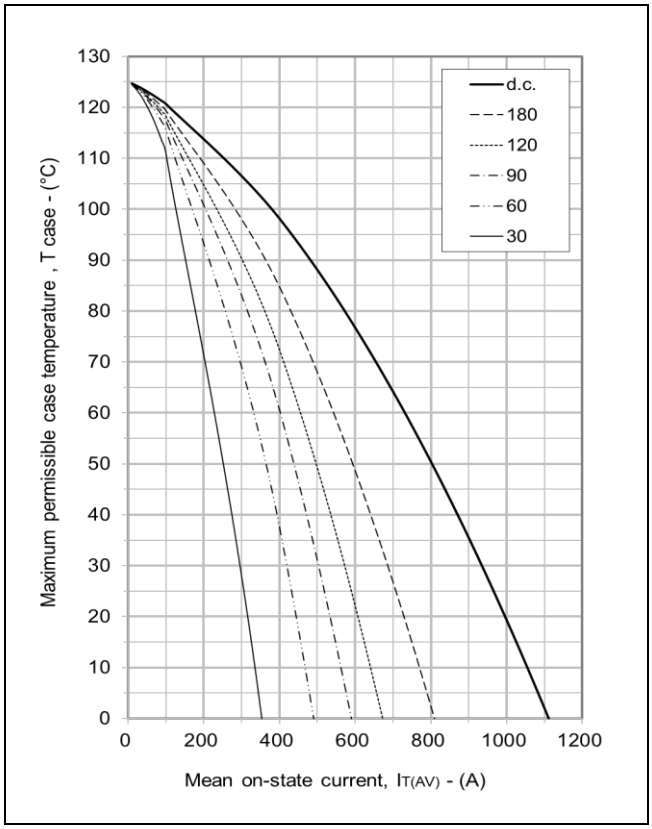


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

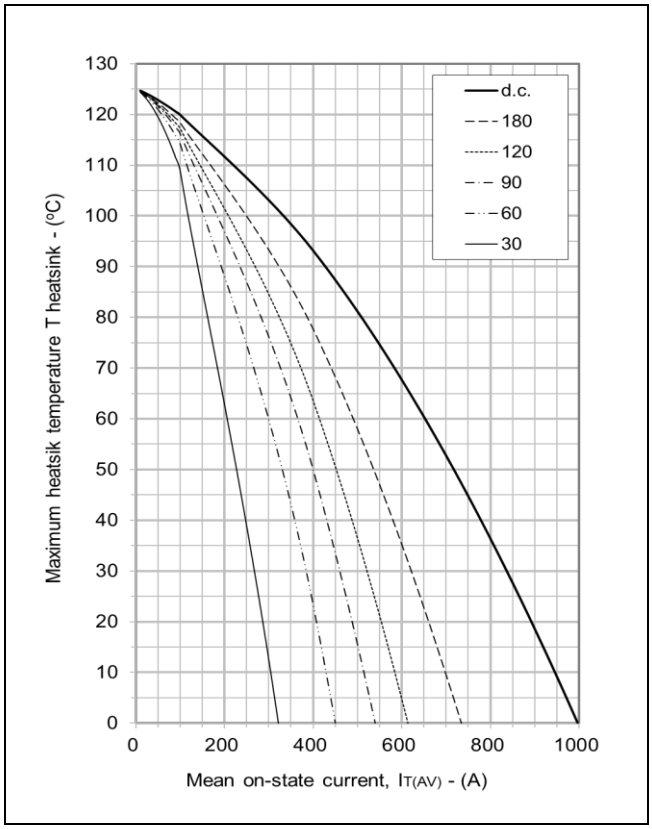
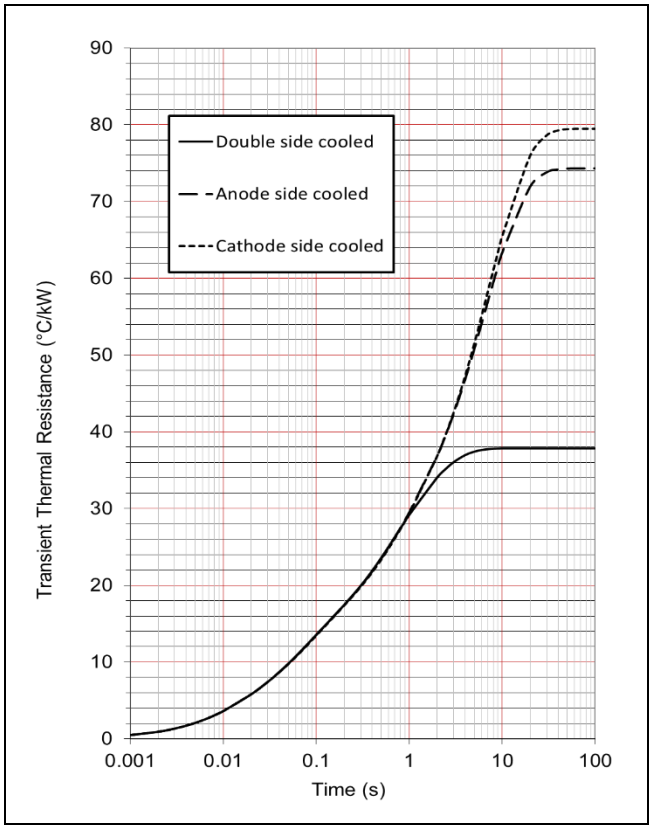


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave



		1	2	3	4
Double side cooled	Ri(°C/kW)	2.426	9.350	10.696	15.376
	Ti(s)	0.009	0.053	0.450	1.395
Anode side cooled	Ri(°C/kW)	2.809	9.558	11.356	50.614
	Ti(s)	0.010	0.059	0.476	6.555
Cathode side cooled	Ri(°C/kW)	2.951	9.403	11.077	56.041
	Ti(s)	0.010	0.061	0.473	7.228

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	$\Delta Z_{th}(z)$	
θ°	sine	rect
180	4.43	3.01
120	5.13	4.30
90	5.89	5.03
60	6.58	5.81
30	7.12	6.67
15	7.36	7.13

Anode Side Cooling		
	$\Delta Z_{th}(z)$	
θ°	sine	rect
180	4.39	2.99
120	5.07	4.26
90	5.81	4.97
60	6.48	5.74
30	7.00	6.57
15	7.24	7.01

Cathode Sided Cooling		
	$\Delta Z_{th}(z)$	
θ°	sine	rect
180	4.37	2.98
120	5.05	4.25
90	5.79	4.96
60	6.45	5.72
30	6.97	6.54
15	7.20	6.98

Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

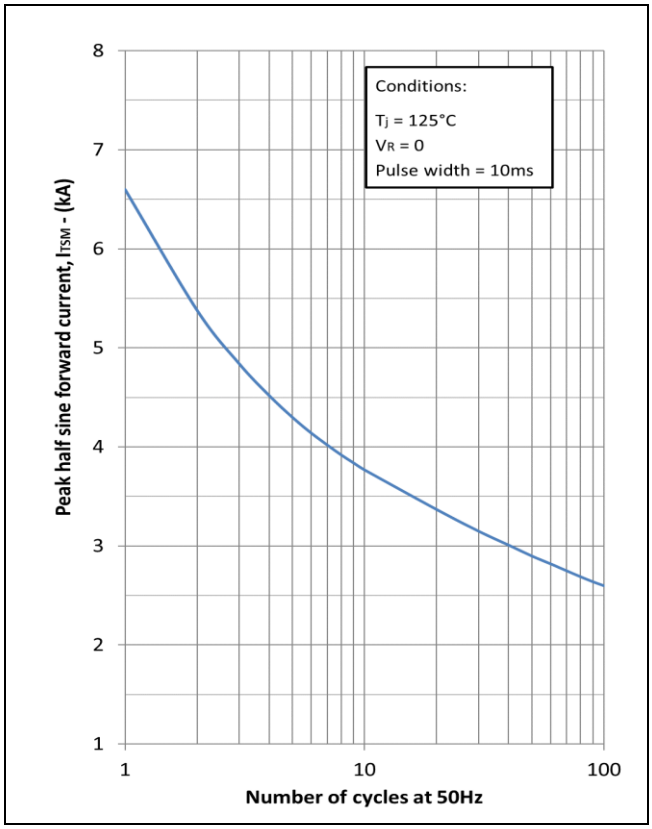


Fig. 10 Multi-cycle surge current

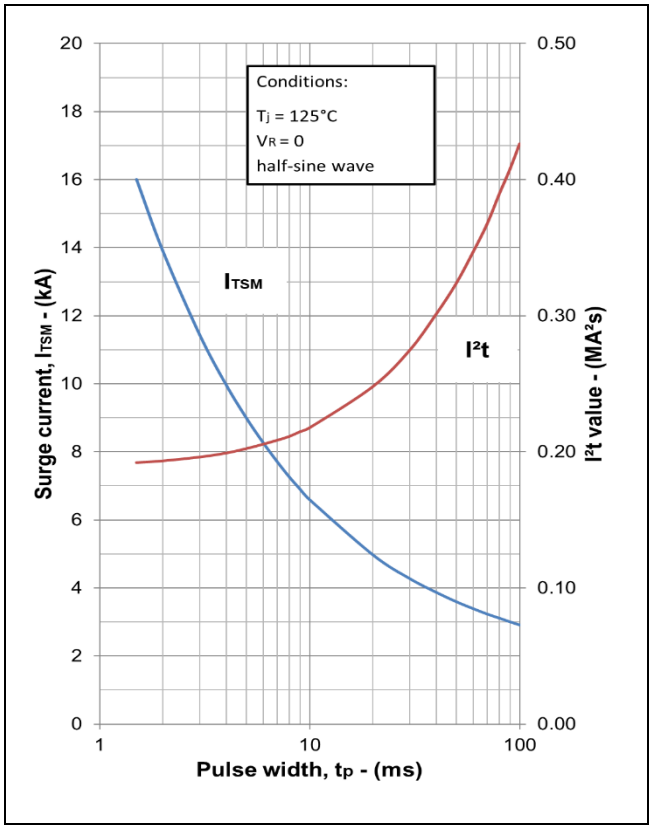


Fig. 11 Single-cycle surge current

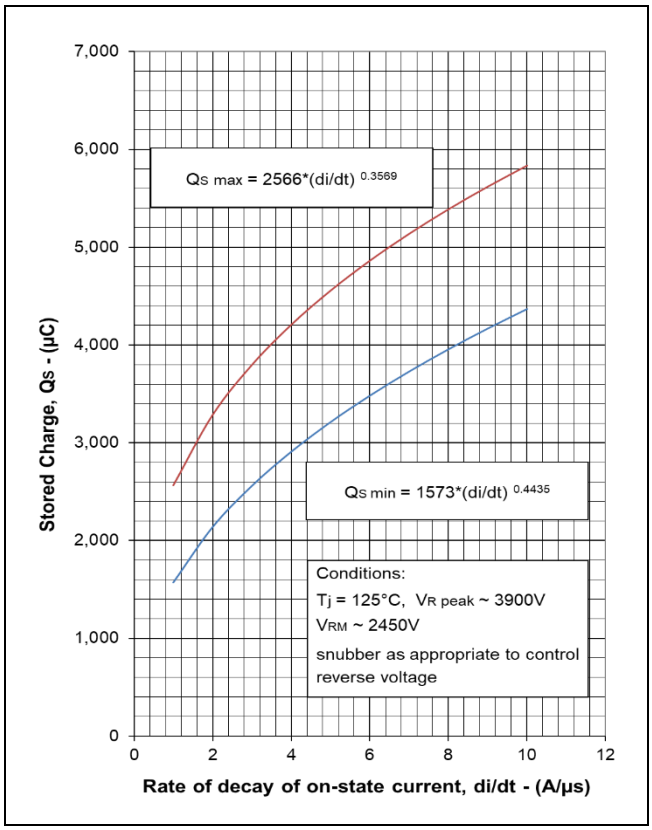


Fig. 12 Stored charge

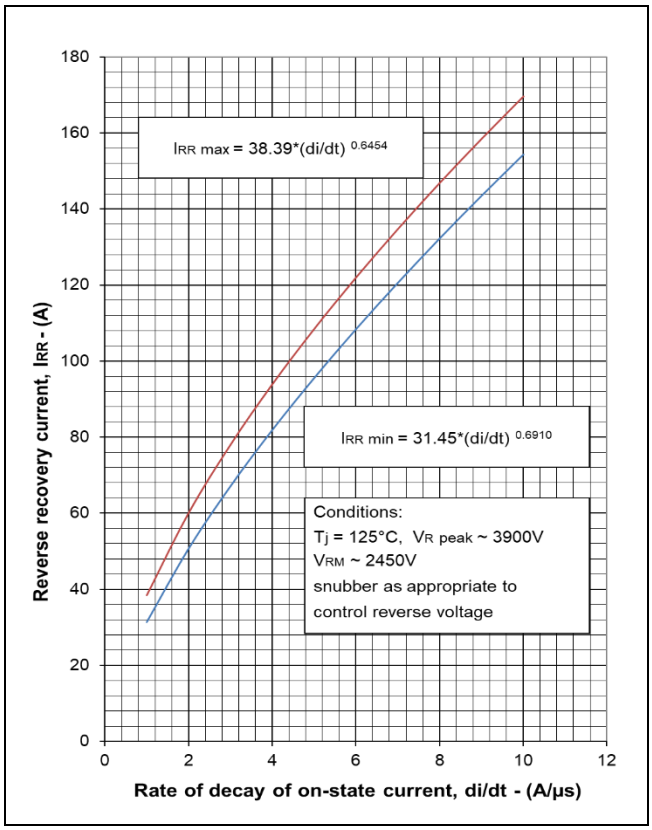


Fig. 13 Reverse recovery current

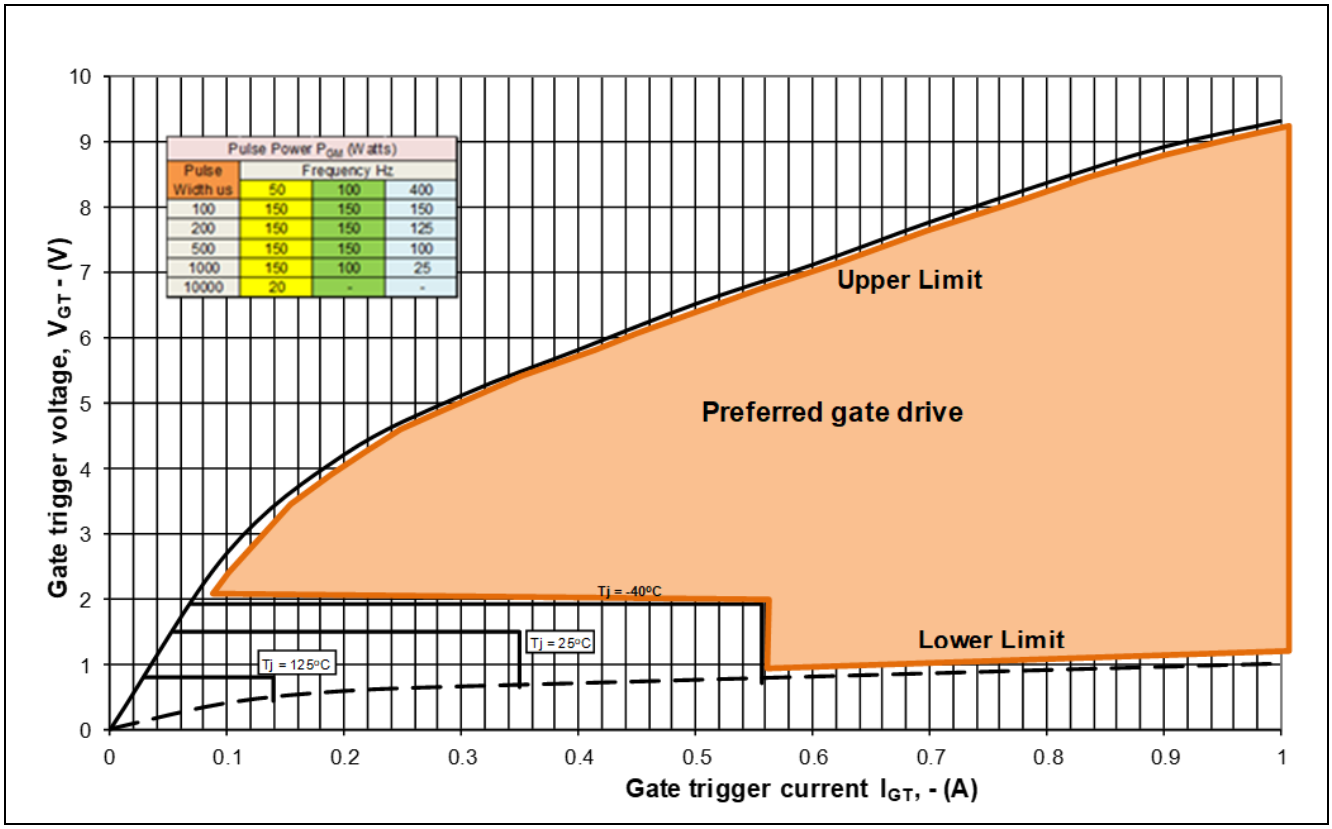


Fig. 14 Gate characteristics

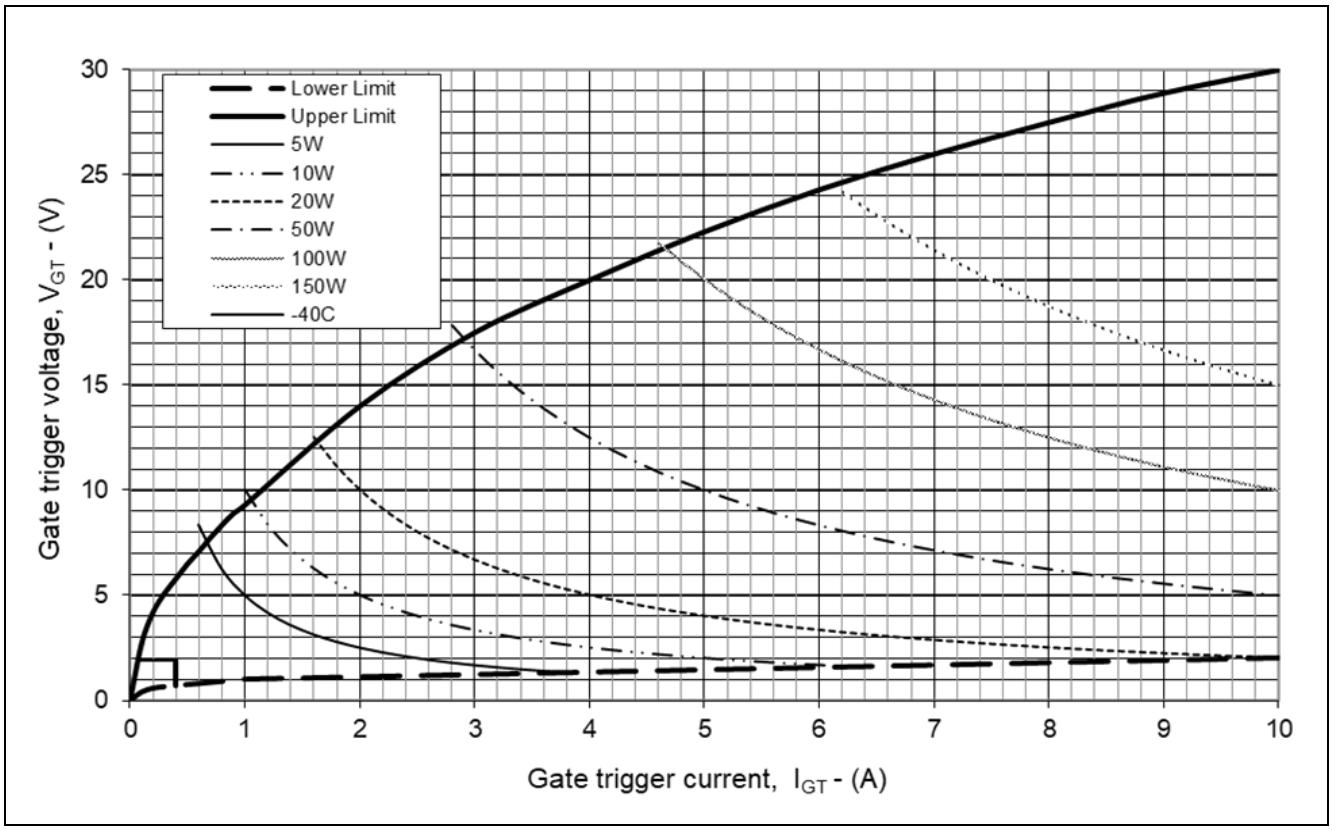


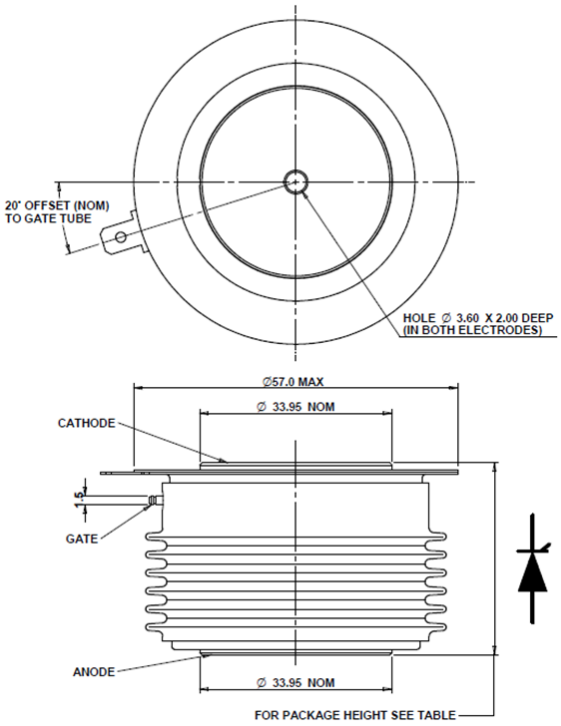
Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR390J85	35.5	35.0
DCR490J65	**35.2**	**34.6**
DCR570J52	34.9	34.4
DCR640J42	34.8	34.2
DCR780J28	34.6	34.0
DCR880J22	34.5	33.9

Lead length: 420mm

Lead terminal connector: M4 ring

Package outline type code: J

Fig. 16 Package outline

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