DCR1110F52

Phase Control Thyristor

Replaces DS5965-3 DS5965-4 December 2023 (LN42953)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

V_{DRM}	**5200V**
$I_{T(AV)}$	**1110A**
I_{TSM}	**14800A**
dV/dt*	**1500V/µs**
dI/dt	**800A/µs**

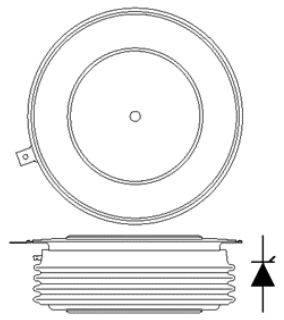
***Higher dV/dt selections are available on request**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
DCR1110F52*	5200	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 100mA, V_{DRM}, V_{RRM} t_p = 10ms V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively
DCR1110F50	5000	

Lower voltage grades available.

*5000V @ -40°C, 5200V @ 0°C



Outline type code: F

(See Package Details for further information)

Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR1110F52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1110	A
$I_{T(RMS)}$	RMS value	-	1740	A
I_T	Continuous (direct) on-state current	-	1690	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C V_R = 0	14.8	kA
I^2t	I^2t for fusing		1.10	MA²s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	18.3	°C/kW
		Single side cooled	Anode DC	-	33.3	°C/kW
			Cathode DC	-	41.7	°C/kW
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 23kN (with mounting compound)	Double side	-	4.0	°C/kW
			Single side	-	8.0	°C/kW
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			20	25	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	100	mA
V_{TM}	Instantaneous forward voltage	At 2900A peak, T_j = 25°C		2.10	2.30	V
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$ Gate source 30V, 10Ω t_r < 0.5µs, T_j = 125°C	Repetitive 50Hz	-	200	A/µs
			Non-repetitive	-	800	A/µs
$V_{T(TO)}$	Threshold voltage - Low level	300A to 800A at T_{case} = 125°C		-	0.92	V
	Threshold voltage - High level	800A to 4000A at T_{case} = 125°C		-	1.08	V
r_T	On-state slope resistance - Low level	300A to 800A at T_{case} = 125°C		-	0.79	mΩ
	On-state slope resistance - High level	800A to 4000A at T_{case} = 125°C		-	0.60	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	T_j = 125°C, V_R = 100V, dI/dt = 5A/µs, dV_{DR}/dt = 20V/µs linear to 2000V		-	1000	µs
Q_S	Stored charge	I_T = 1000A, t_p = 1000µs, T_j = 125°C, dI/dt = 5A/µs. [LEM]		2200	3800	µC
I_{RR}	Reverse recovery current			90	115	A
Q_S	Stored charge	T_j = 125°C, dI/dt = 1A/µs, $V_{R\ peak}$ ~ 3000V, V_R ~ 2200V		**(Typ.)** 1680		µC
I_{RR}	Reverse recovery current			**(Typ.)** 33		A
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	350	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	10	mA

CURVES

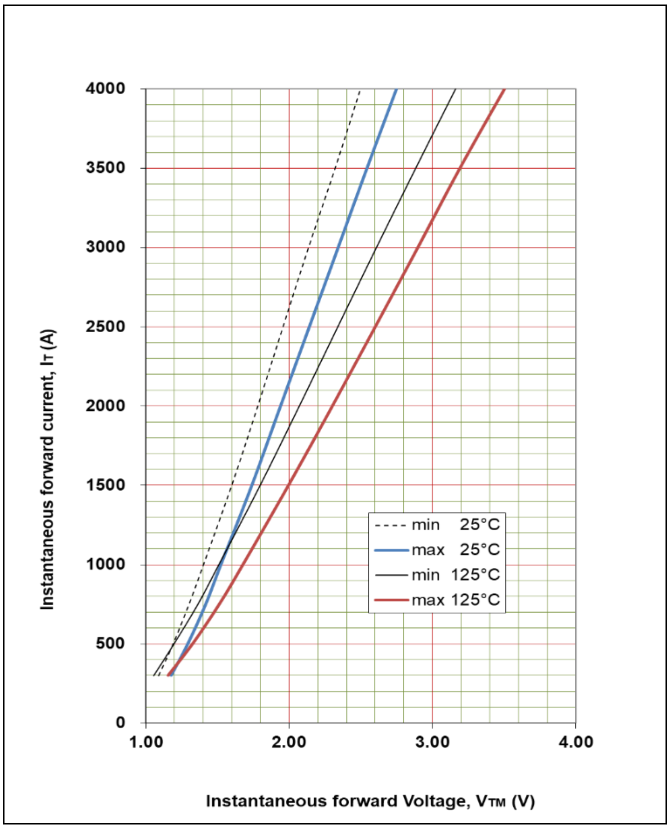


Fig. 2 Maximum & minimum on state characteristics

V_{TM} EQUATION

$V_{TM} = A + B.\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = -0.070068
B = 0.224191
C = 0.000656
D = -0.014462

These values are valid for T_j = 125°C for I_T 300A to 4000A

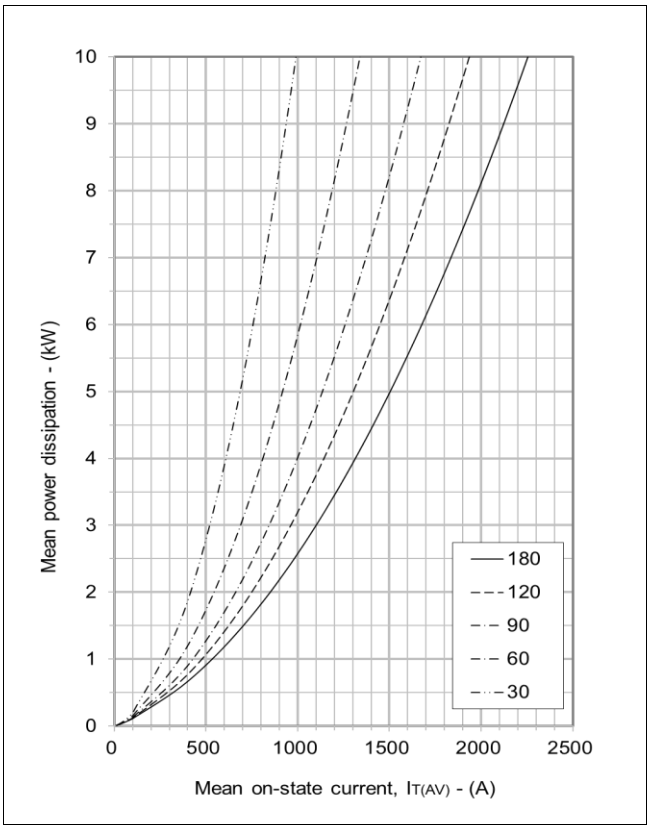


Fig. 3 On-state power dissipation - sine wave

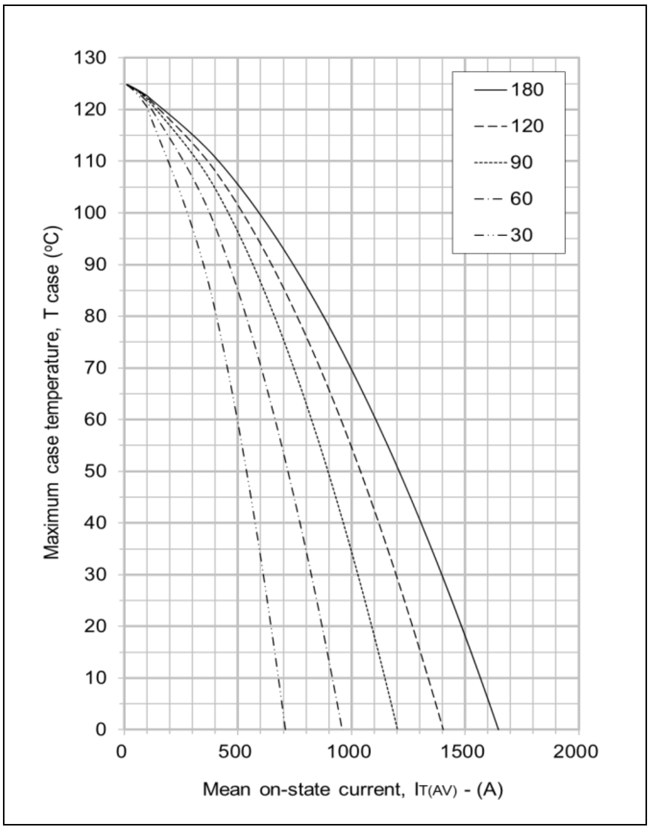


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

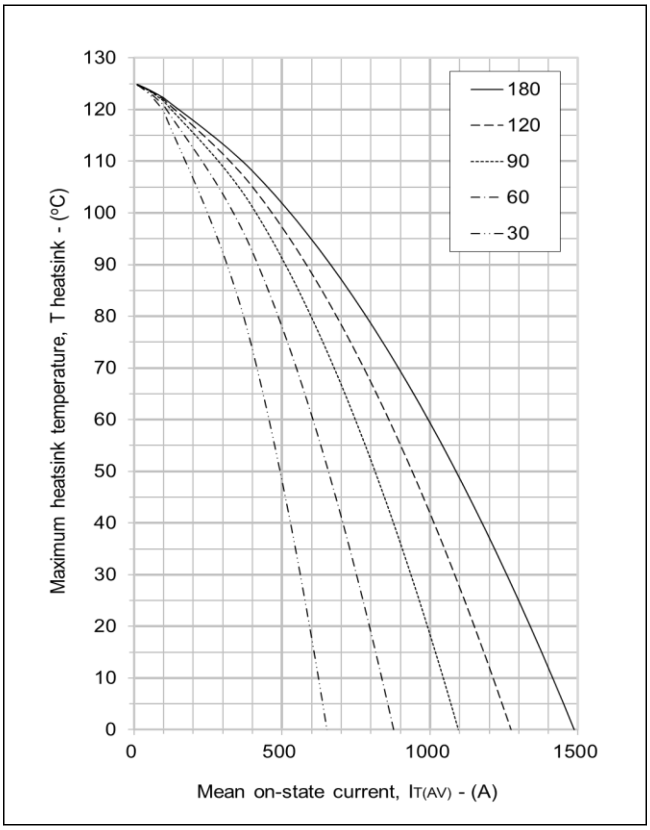


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

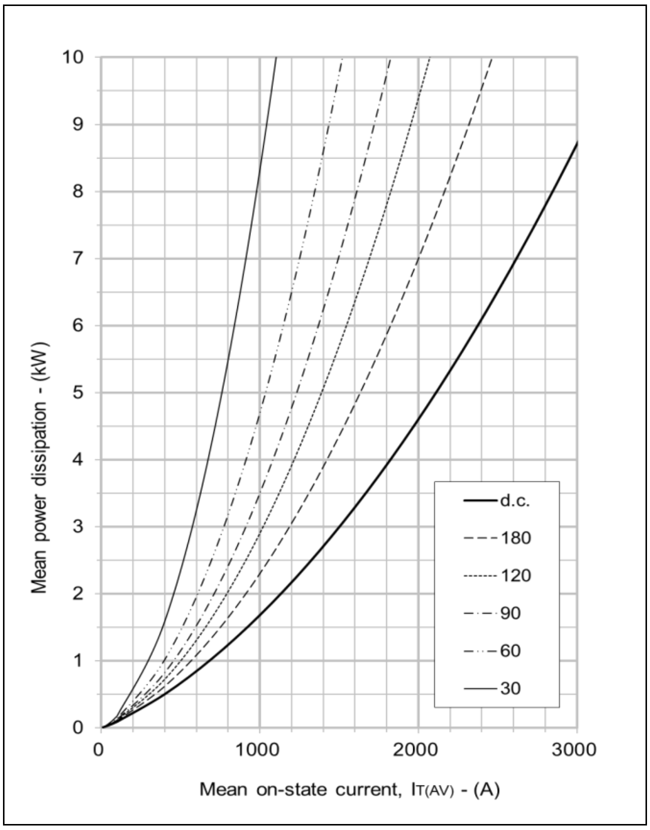


Fig. 6 On-state power dissipation - rectangular wave

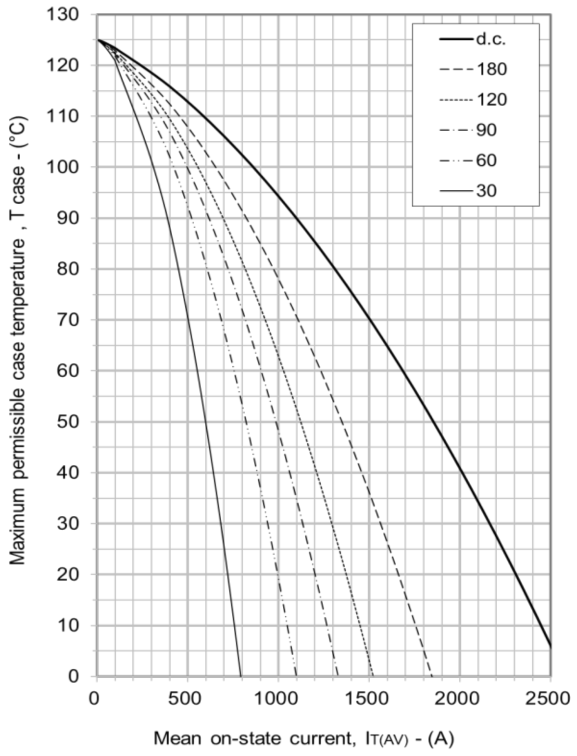


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

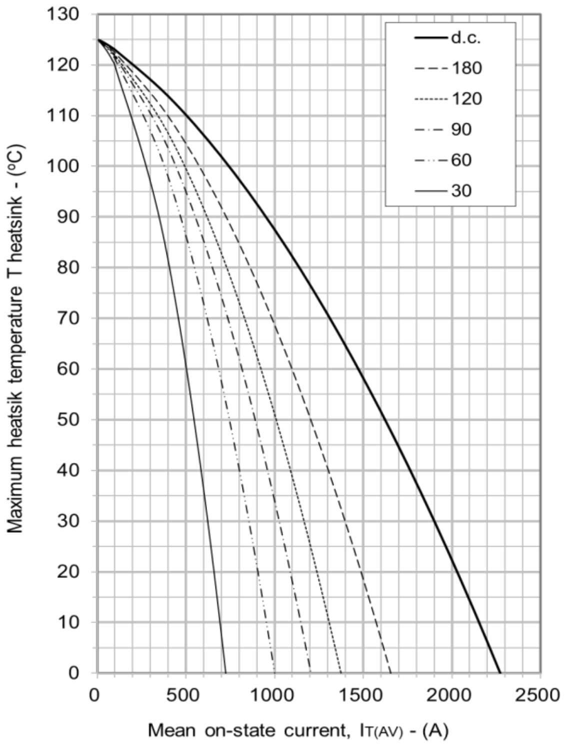
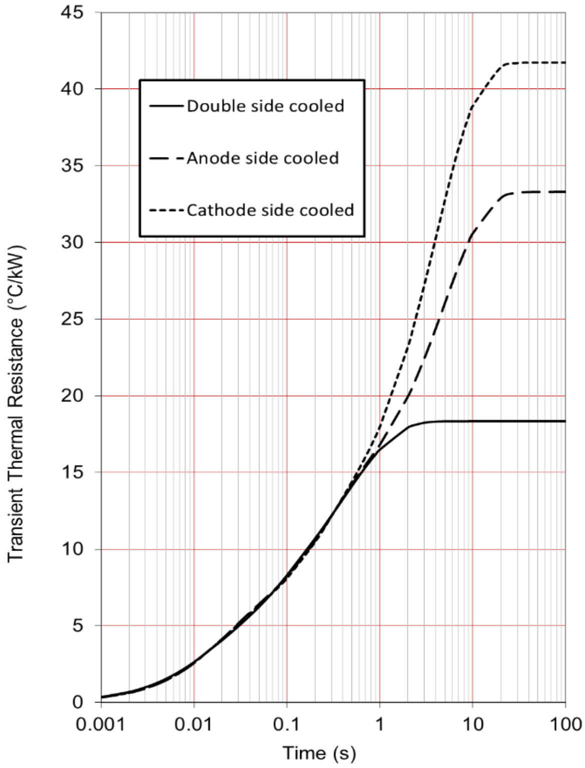
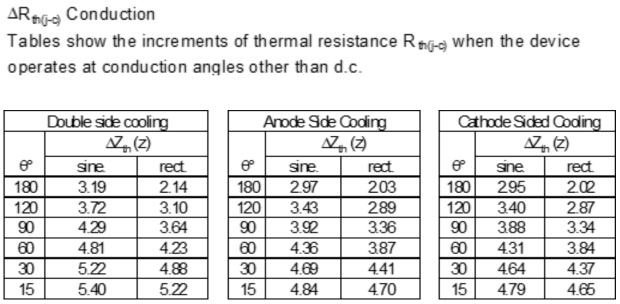


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave



		1	2	3	4
Double side cooled	Ri(°C/kW)	7.561	4.077	3.842	2.867
	Ti(s)	0.688	0.254	0.061	0.010
Anode side cooled	Ri(°C/kW)	11.556	8.581	4.794	8.364
	Ti(s)	4.222	6.027	0.017	0.226
Cathode side cooled	Ri(°C/kW)	6.721	4.622	15.539	14.863
	Ti(s)	0.191	0.016	5.001	3.317

$$Z_{th} = \sum_{i=1}^{i=4} R_i \,.\left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$



$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	3.19	2.14
120	3.72	3.10
90	4.29	3.64
60	4.81	4.23
30	5.22	4.88
15	5.40	5.22

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	2.97	2.03
120	3.43	2.89
90	3.92	3.36
60	4.36	3.87
30	4.69	4.41
15	4.84	4.70

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	2.95	2.02
120	3.40	2.87
90	3.88	3.34
60	4.31	3.84
30	4.64	4.37
15	4.79	4.65

Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

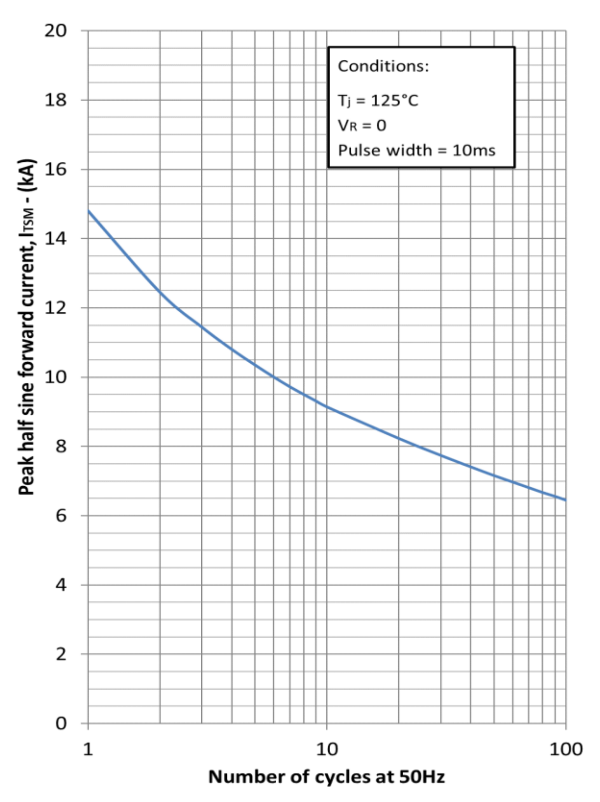


Fig. 10 Multi-cycle surge current

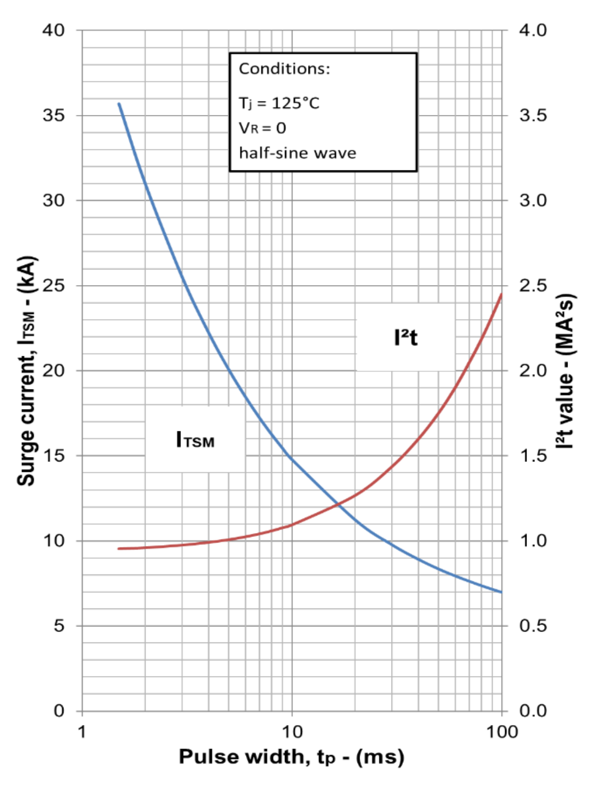


Fig. 11 Single-cycle surge current

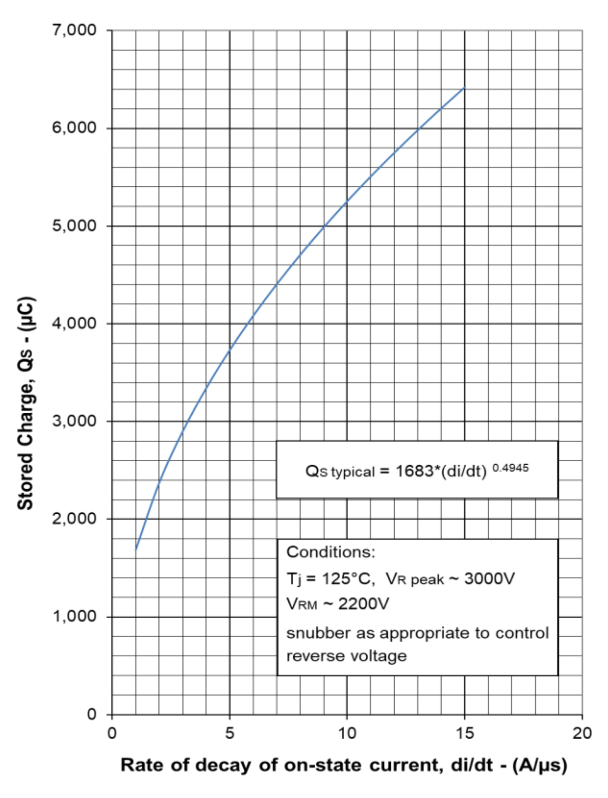


Fig. 12 Stored charge

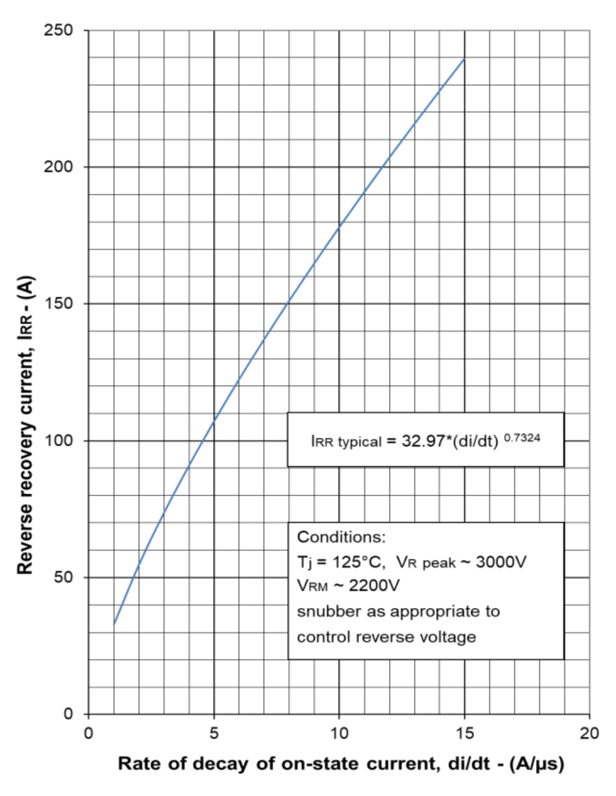
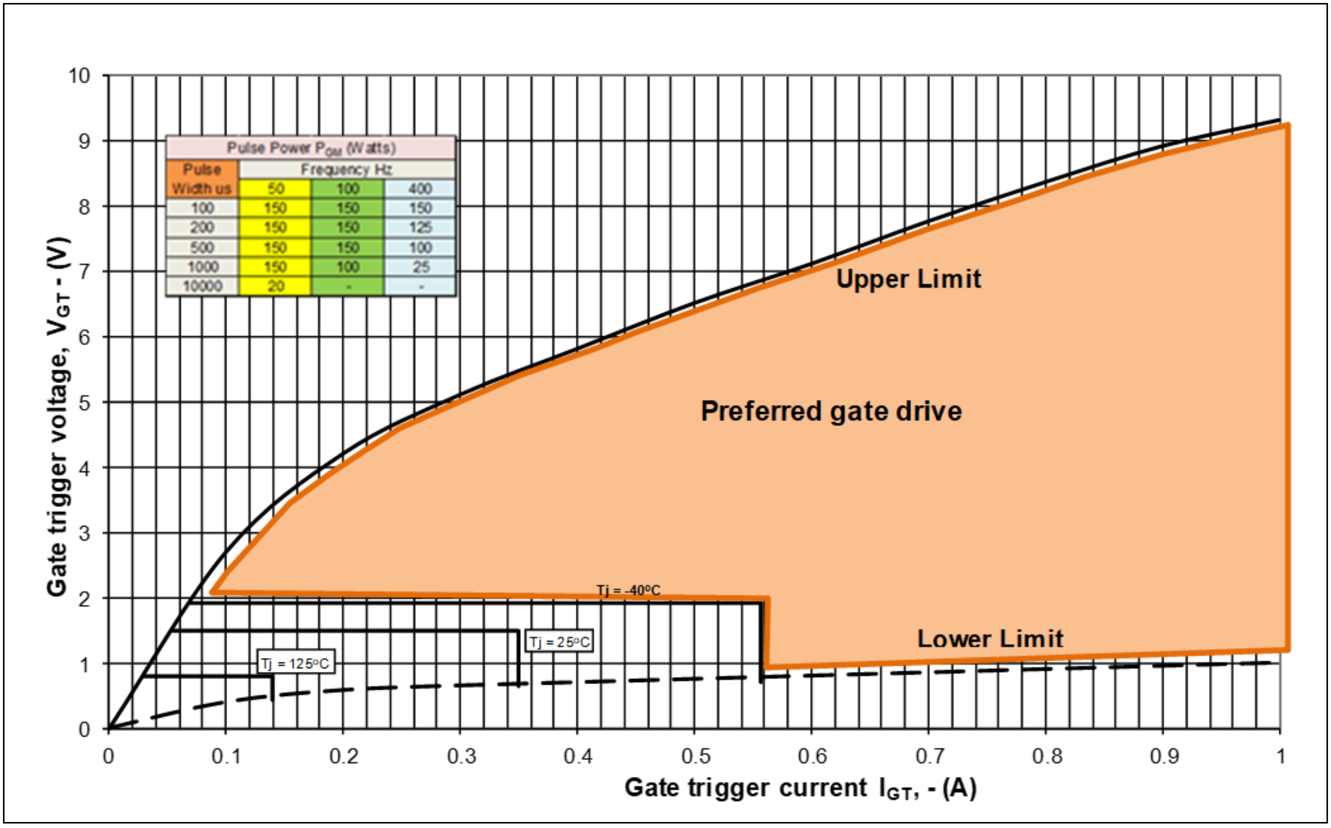


Fig. 13 Reverse recovery current



Pulse Power P_{GM} (Watts)			
Pulse Width us	Frequency Hz		
	50	100	400
100	150	150	150
200	150	150	125
500	150	150	100
1000	150	100	25
10000	20	-	-

Fig. 14 Gate characteristics

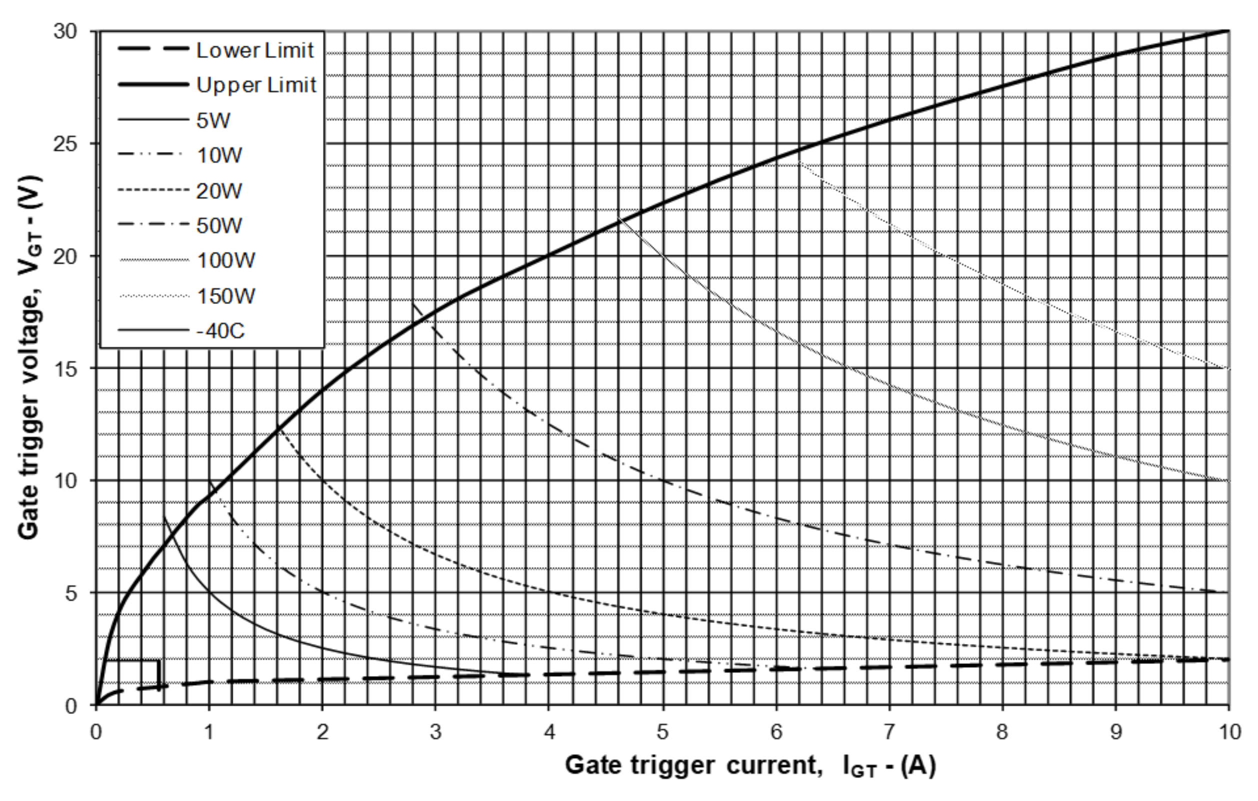


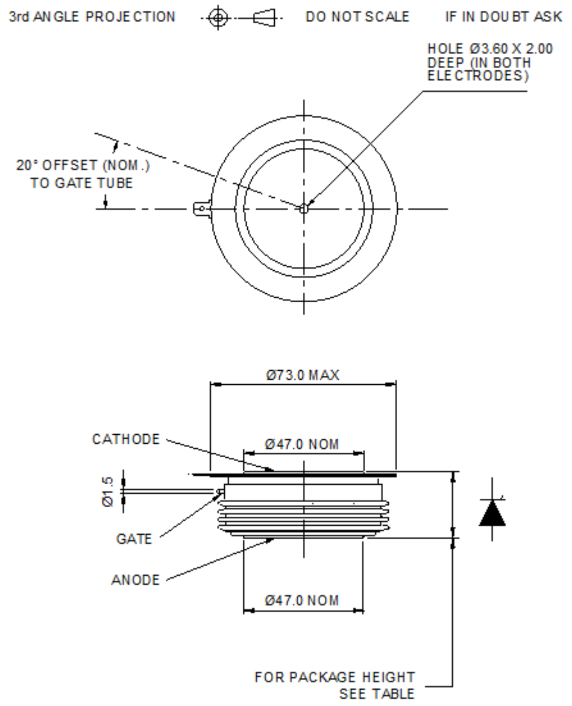
Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR750F85	27.4	26.9
DCR890F65	27.1	26.6
DCR1110F52	**26.9**	**26.3**
DCR1260F42	26.7	26.2
DCR1610F28	26.5	26.0
DCR1770F22	26.4	25.9

Lead length: 420mm

Lead terminal connector: M4 ring

Package outline type code: F

Fig. 16 Package outline

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