AN 5950

Understanding i^2 Phase Control Thyristor Datasheets

Application Note

AN5950-1 Sept 2009 LN26885

Authors: Dinesh Chamund, Colin Rout

INTRODUCTION

This note will guide you through the Dynex i^2 Phase Control Thyristor data sheet format and explain its contents. For the purpose of discussion and illustration, Dynex datasheet for the DCR3030V42 has been chosen and its contents explained in sequence starting from the first page.

The i^2 Phase Control Thyristor datasheet includes tables and graphs of data regarding device ratings and characteristics. In order to use the datasheet properly it is important that the user has a good understanding of the information presented in the datasheet. Also when benchmarking with similar product from a different supplier, allowance should be made for any difference in the way the parameters are defined, specified and measured. Hopefully this will promote an efficient and reliable use of the device and also help the user to make a correct choice of device for the intended application.

The datasheet is organised in the following sections:

- PART NUMBER
- FEATURES
- APPLICATIONS
- TABLE OF VOLTAGE RATINGS
- ORDERING INFORMATION
- KEY PARAMETERS/PACKAGE OUTLINE
- TABLES OF RATINGS
  - CURRENT RATINGS
  - SURGE RATINGS
  - THERMAL AND MECHANICAL RATINGS
- TABLES OF CHARACTERISTICS
  - DYNAMIC CHARACTERISTICS
  - GATE CHARACTERISTICS
- CURVES
- PACKAGE DETAILS

PART NUMBER

DCR3030V42

The part numbering scheme for the Dynex i^2 Phase Control Thyristor is as follows:

DCR = **D**ynex **C**ontrol **R**ectifier

3030 = Headline average current rating (A)

V = Package code

42 = Maximum repetitive voltage rating (V)/100

A Dynex datasheet is a controlled document with a specific document number, issue number, and date. This information appears below the device type in the header on the right hand side of the first page . Dynex reserves the right to change the data without notice and so the users are advised to refer to the latest version by visiting Dynex web site: http://www.dynexsemi.com

KEY PARAMETERS/PACKAGE OUTLINE

This is a summary of main parameters unique to the part number. The full description of these parameters is found with appropriate test conditions in the main body of the

datasheet. It is important that when comparing the key parameters with other similar product a full description of the parameters should be considered as manufacturers often specify different test conditions.

Fig.1 gives the package outline and its code (V).

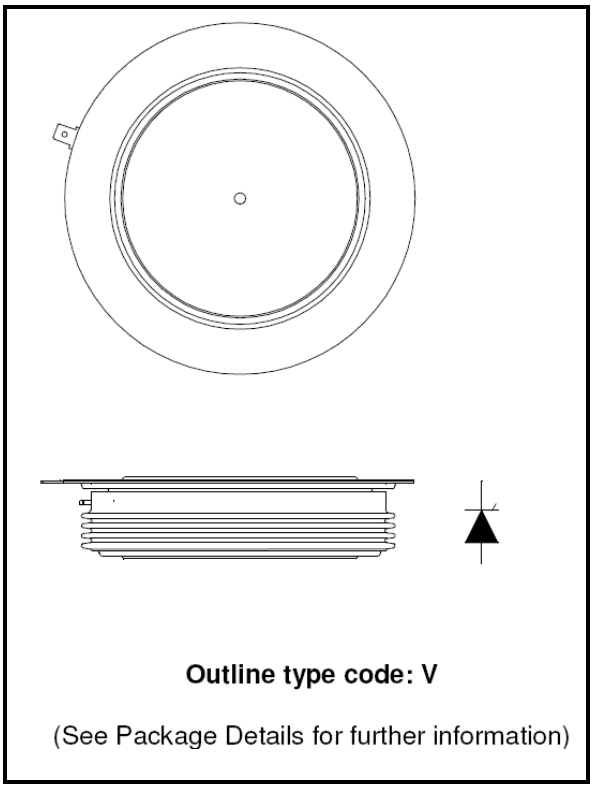


Fig. 1 Package outline

FEATURES

The features section provides a list of specific key attributes of the device design and technologies.

APPLICATIONS

A few examples of possible application are indicated here. It should be noted that inclusion in this section does not imply that Dynex has fully tested the device under all application conditions. The suitability of a device for a given application rests solely with the user.

TABLE OF VOLTAGE RATINGS

This table provides the repetitive peak voltage ratings of the device given under specified conditions.

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR3030V42 DCR3030V40 DCR3030V35 DCR3030V30	4200 4000 3500 3000	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 200mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

V_{DRM}, V_{RRM} are the peak repetitive voltages in the (direct) forward and reverse directions. The rating is for 50Hz half sine waves of voltage and assumes that the device is maintained at the maximum rated junction temperature of 125°C by suitable heatsinking, if required. V_{DRM} & V_{RRM} are the voltages that the device reaches when the leakage currents I_{RDM} &I_{RRM} reach their test limits as given in the datasheet, or the maximum rated voltage whichever is reached first. The device may well be capable of reaching a higher voltage but excessively large leakage currents will make temperature control difficult and failure through thermal run-away may occur for all but the shortest pulses.

As the temperature of the device is reduced, the natural avalanche voltage of the silicon wafer reduces. In some cases, at very low temperatures and at the lower limit of the tolerance on the silicon specification the full voltage rating of the device may not be achieved. Where this is the case, this is annotated on the datasheet.

Because of transient voltage spikes generated by switching devices on the supply, thyristors are usually operated at nominal peak line voltages of V_{DRM} divided by a safety factor of 1.5 to 2.5, depending on the transient voltages. A low safety factor is used when the

transients are largely determined, usually in the case of self commutated converters with large energy storage elements. If the transients on the mains supply are unknown then a safety factor of 2 to 2.5 should be used.

V_{DSM} & V_{RSM} are the peak non-repetitive voltages in the forward and reverse directions and are the voltages that can be applied occasionally and non-repetitively and should not be exceeded under any circumstances.

ORDERING INFORMATION

This specifies the correct part number for ordering the device, for example:

DCR3030V42 (4200V part)

Other voltage grades can be selected as given in the table of voltage ratings.

TABLES OF RATINGS

- CURRENT RATINGS

$I_{T(AV)}$ – Mean on-state current

$I_{T(AV)}$ is the average value of a half sine wave current flowing in a thyristor such that the peak junction temperature is limited to the rated temperature of 125°C with the case temperature specified. The average current rating of the device is related to the thermal rating of the device package and thus by equating the power generated within the device to the power dissipated in the package, the average current rating can be calculated. A more thorough analysis of the current rating derivation is given in the Appendix 1.

There is no industry standard definition for $I_{T(AV)}$, manufacturers quote $I_{T(AV)}$ with case temperatures of 60°C, 65°C, 70°C and 85°C . Others quote with respect to a heatsink temperature of 55°C (see Fig.17 Appendix 1). Thus direct comparison of headline ratings is very difficult. Even if all manufacturers quoted at the same case temperature this would still not resolve the problem because, in reality, what is really important in the application is how the device performs on the heatsink. Some manufacturers quote low values of thermal resistance junction to case with correspondingly higher values for thermal resistance case to heatsink but with similar thermals junction to heatsink. Therefore their headline $I_{T(AV)}$ at a given case temperature may be quoted as being higher than competitors' devices but when rated on the same heatsink there is no appreciable difference in performance.

Dynex quotes a headline $I_{T(AV)}$ at 60°C case temperature but gives full de-rating curves for both half sine and rectangular waves to enable the user to make direct and meaningful comparisons.

$I_{T(RMS)}$ – RMS current rating

For today's capsule devices $I_{T(RMS)} = \pi . I_{T(AV)}/2$. Historically $I_{T(RMS)}$ could have been different because, for single sided devices with a flexible lead for the load current terminal, the current carrying capability of the connections could be less than the capability of the silicon. For capsule (puk) devices, the cross sectional area of the electrodes is the same as the silicon so no allowance needs to be made. The limitation is now the equipment busbars.

I_T – Continuous (direct) on-state current

I_T is the maximum continuous current that the thyristor can conduct while maintaining the junction temperature to its maximum rated value of 125°C. Note that, like $I_{T(AV)}$, this figure depends upon the stated reference case temperature.

- SURGE RATING

I_{TSM} – Surge (non-repetitive) on-state current

I_{TSM} is the maximum 10ms half sine wave of current, following maximum load current (i.e. the thyristor junction temperature is at $T_{j\ max}$) that the thyristor can conduct without the device experiencing thermal run-away and the silicon melting. I_{TSM} is determined by the manufacturer by viewing the forward voltage characteristic of the thyristor at high currents and observing the onset of thermal run-away. Exceeding this limit will damage the device and the rating should only be used for the selection of fuses. Because the device is so hot following the surge current pulse it loses its ability to block voltage, this rating is for zero reverse re-applied voltage. Also the temperature excursion is so high that the device will fail due to temperature cycling wear out if this level of current is repeated several times in the life of the device. In practice, Dynex derates the surge current limit of its i^2 thyristors by 10% which means that the device can survive about 100 occurrences of the stated current in its life.

I^2t – for fusing

I^2t for fusing is $\int i^2dt$ and is calculated for a half sine wave as

I^2_{TSM}.base width/2

As well as the single 10 ms half sine wave rating, Dynex gives a graph showing the ratings for shorter and longer pulses of current with the corresponding I^2t values; figure 11 of the datasheet. These are derived by calculating the current that gives the same peak temperature as the 10ms half sine wave derived from the physical rating of the device. Again 100 occurrences in the life of the device are permissible.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3030	A
$I_{T(RMS)}$	RMS value	-	4760	A
I_T	Continuous (direct) on-state current	-	4550	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	40.6	kA
I^2t	I^2t for fusing	V_R = 0	8.24	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00746	°C/W
		Single side cooled	Anode DC	-	0.0130	°C/W
			Cathode DC	-	0.0178	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 54kN	Double side	-	0.002	°C/W
		(with mounting compound)	Single side	-	0.004	°C/W
T_{vj}	Virtual junction temperature	(blocking)		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			48.0	59.0	kN

- THERMAL AND MECHANICAL RATINGS

$R_{th(j-c)}$ – Thermal resistance – junction to case

The thermal resistance enables the calculation of the temperature rise of the silicon in the device above the external case temperature. It has the dimensions of °C/W or K/W. In other words, if the device is generating DC power losses P, then the temperature rise of the junction above the case temperature is P x $R_{th(j-c)}$. Values of the thermal resistance are given for double side cooling and cooling via either the anode or cathode electrode.

$R_{th(c-h)}$ – Thermal resistance – case to heatsink

Of course the reference point for temperature rise for the user is the ultimate cooling medium air, water, oil etc. The total thermal resistance will include the thermal resistance of the heat sink (fin) to ambient, which is the user's design choice and the contact thermal resistance between the device contact surface and the heat sink (Fig. 17 Appendix 1). This resistance depends upon the quality of the interface and the value quoted is with the inclusion of a good quality thermally and electrically conductive compound and with the joint clamped to the median recommended force.

T_{vj} – Virtual junction temperature

The device junction temperature cannot be directly measured but is usually calculated from a measured reference temperature e.g. case or heat sink using the product of thermal resistance value and the power dissipation. Hence it is referred to as the virtual junction temperature. The maximum value of T_{vj} is limited by the blocking capability of the device. This is set at 125°C. If this limit is exceeded then the subsequent reliability of the device operation cannot be guaranteed.

T_{stg} – Storage temperature range

During the storage of the device there are no application stresses applied (blocking stress, power losses etc) and hence the storage temperature range is determined purely by the withstand capability of the materials used

in the construction of the device. The storage temperature range is conservatively set at -55°C to 125°C.

F_m – Clamping force

Correct clamping of the device is necessary to assure the electrical and thermal contact to the active part of the device. The recommended maximum and minimum force is stated for each device type (see Appendix 3 and Application note AN4839).

- DYNAMIC CHARACTERISTICS

I_{RRM}/I_{DRM} – Peak reverse and off-state current

I_{RRM} and I_{DRM} are the maximum blocking currents when V_{RRM} and V_{DRM} are applied to the device respectively. These currents are temperature dependant and specified at T_{case} = 125°C and tp= 10ms. Note that for high voltage devices the blocking current can contribute substantially to the power losses.

dV/dt – Maximum Linear rate of rise of off-state voltage

This is the maximum value for the linear rate of rise of forward voltage (from 0V to 67%V_{DRM}) that can be applied without initiating turn-on in the thyristor with the gate open circuit. It is not advisable to exceed this value as it will cause uncontrolled turn-on in the device and may cause damage. It is usual practice to protect the device against excessive values of dV/dt by use of an additional snubber circuit (RC or RCD snubber circuit). The dV/dt capability of a thyristor reduces with increasing temperature. This is because triggering of the thyristor is initiated by the sum of the junction leakage current, the Cdv/dt displacement current and the gate current. dV/dt is specified at T_{case} = 125°C which should be the worst case.

dI/dt – Rate of rise of on-state current

This is the maximum rate of rise of on-state current (load current) for which two values are specified; repetitive @50Hz and non-repetitive. These values are specified under the conditions of forward blocking voltage of 67%V_{DRM}, peak forward current of twice the rated average current ($2xI_{T(AV)}$), T_j = 125°C and the gate conditions for each device type (gate source voltage, gate resistance and the gate current rise time). When a thyristor is triggered on the initial conduction area is small and hence the current carrying capacity is limited. If the dI/dt rating is exceeded then damage to the thyristor may occur. It is advisable to control the dI/dt of the load current by use of turn-on snubber circuit (usually a clamped reactor). Note that the dI/dt snubber discharge current should be included in dI/dt considerations.

$V_{T(TO)}$ – Threshold voltage

For a simple calculation of conduction losses of a thyristor, the on state IV characteristic is approximated to a straight line and an intercept on the voltage - axis. The intercept is called the threshold voltage. Two values of $V_{T(TO)}$ are given on the datasheets to give more accurate approximations by splitting the IV curve into a low level current range and a high level current range.

r_T – On-state slope resistance

The straight line in the above approximation is also defined by a slope (dI_T/dV_T) = $1/r_T$ where r_T is called the slope resistance (dV_T/dI_T). Once again r_T is specified for low and high level current range respectively.

A full explanation of how $V_{T(TO)}$ and r_T are derived is given in the Appendix 2.

t_{gd} – Delay time

This is the gate controlled delay time defined as the time interval during turn-on between 10% of the peak gate current I_{GT} and 90% of the anode voltage V_D (see Fig.22 in Appendix 4). The value is specified under the conditions of V_D = 67%V_{DRM}, T_j = 125°C, and gate conditions for the given thyristor (gate source = 30V, 10Ω and t_r = 0.5µs).

t_q – Turn-off time

The turn-off time t_q is defined as the time interval between the anode current reaching zero value after the conduction period and when the thyristor can withstand reapplied positive anode voltage (see Fig. 23 Appendix 5). Assuming the dI/dt is slow then t_q is a function of T_{vj}, dI/dt, and dV/dt (see Figures 26, 27 and 28 in Appendix 6). t_q is specified under the conditions of T_j = 125°C, V_R = 200V, dI/dt = 1A/µs, and dV_{DR}/dt = 20V/µs linear.

Q_S – Stored charge

This is defined as the time integral of the reverse recovery current which flows when a thyristor is reverse biased after forward conduction (see Fig. 23 Appendix 5). The value of Q_S is specified at T_j=125°C, the falling rate of current (- dI/dt), reverse peak voltage V_{Rpk}, and the reverse blocking voltage V_{RM}. The measurement is done with a suitable RC snubber circuit to limit the peak voltage to the specified limit. For practical reason the integral is taken over the first 150µs of recovery. Note that Q_S has the same meaning as Q_{rr} (reverse recovery charge) used elsewhere. Q_s is a function of dI/dt (Fig.12) and T_{vj} (Fig. 24 in Appendix 6) assuming dI/dt is slow.

I_L – Latching current

The latching current is the minimum anode current required to maintain the thyristor in forward conduction state after turn-on has been initiated and the gate signal is then removed. Therefore the gate trigger current should be maintained or repeated until the anode current reaches this value under all conditions.

I_H – Holding current

The holding current is the minimum anode current required to sustain the thyristor in conduction after latching. The thyristor will turn-off suddenly if the current through the thyristor drops below the holding current. For this reason care should be taken to eliminate oscillations at low value of anode current.

- GATE TRIGGER CHARACTERISTICS AND RATINGS

V_{GT} – Gate trigger voltage

This defines the minimum gate voltage required to trigger the thyristor. The V_{GT} is specified at V_{DRM} = 5V and T_{case} = 25°C when the thyristor is most immune to triggering.

V_{GD} – Gate non-trigger voltage

The gate non-trigger voltage is defined as the maximum gate voltage which will not trigger the thyristor. It is specified at V_{DRM} and T_{case} = 125°C when the thyristor is most sensitive to triggering.

I_{GT} – Gate trigger current

This defines the minimum gate current required to trigger the thyristor. I_{GT} is a function of anode to cathode voltage and junction temperature. In the datasheet I_{GT} is specified at V_{DRM} = 5V and T_{case} = 25°C.

I_{GD} – Gate non-trigger current

The gate non-trigger current is the maximum gate current which will not trigger the

thyristor and is specified at V_{DRM} and T_{case} = 125°C.

Note that both V_{GD} and I_{GD} ratings are important when operating a thyristor in a "noisy" environment where it is possible to trigger the thyristor spuriously. Any uncontrolled triggering of the thyristor can lead to malfunction of the circuit operation and possible damage to the device.

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	400	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	200A to 1700A at T_{case} = 125°C		-	0.82	V
	Threshold voltage – High level	1700A to 7000A at T_{case} = 125°C		-	0.98	V
r_T	On-state slope resistance – Low level	200A to 1700A at T_{case} = 125°C		-	0.292	mΩ
	On-state slope resistance – High level	1700A to 7000A at T_{case} = 125°C		-	0.198	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		TBD	TBD	µs
t_q	Turn-off time	T_j = 125°C, V_R = 200V, dI/dt = 1A/µs, dV_{DR}/dt = 20V/µs linear		250	500	µs
Q_S	Stored charge	T_j = 125°C, dI/dt – 1A/µs, $V_{R\,pk}$ =3000V, V_{RM}= 1700V		1600	3500	µC
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At V_{DRM}, T_{case} = 125°C	TBD	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	250	mA
I_{GD}	Gate non-trigger current	V_{DRM} = 5V, T_{case} = 25°C	TBD	mA

CURVES

Maximum and minimum on-state characteristics:

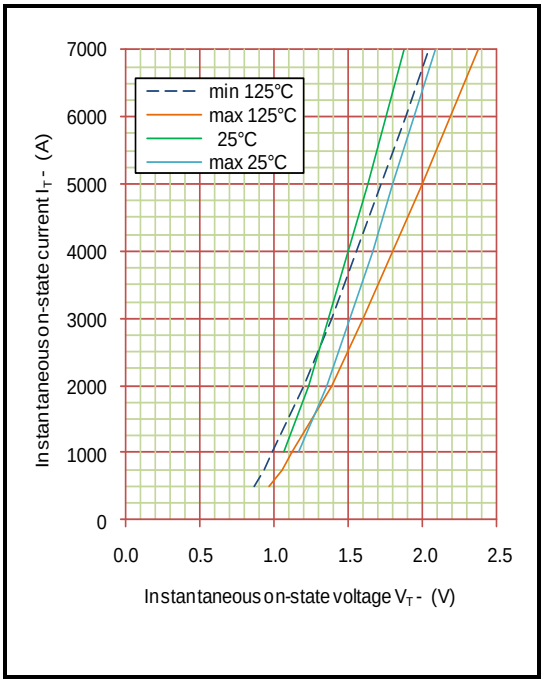


Fig.2 Maximum & minimum on-state characteristics

Fig. 2 shows the graph of maximum and minimum on-state characteristics of the thyristor when it is in full conduction. The instantaneous on-state currents and voltages are plotted against each other at temperature of 25°C and 125°C. These characteristics are used for calculation of on-state power losses. To facilitate the use of a computer for these calculations, an analytical model equation is also given for the voltage drop as a function of current for a specified temperature. The model is valid for a given range of thyristor current and T_j = 125°C (isothermal operation). The voltage drop model used here is:

$$V_{TM} = A + B \times \ln(I_T) + C \times I_T + D \times \sqrt{I_T}$$

where A, B, C and D are the constants of the curve fit of the equation to the measured values. Note that in the model V_{TM} is a function of I_T alone because isothermal operation (no self heating due to device loss) is assumed for the given current range. Also note that in contrast to the linear model using V_{TO} and r_T this model gives an accurate estimation of conduction losses over the entire quoted current range.

On-state power dissipation

Fig.3 and Fig.6 show maximum on-state power dissipation as a function of mean on-state current $I_{T(AV)}$ for sinusoidal and rectangular waves respectively. These are based on the maximum on-state characteristics at 125°C in Fig.2. A family of curves is given for conduction angles ranging from 30° to 180° and DC. The power loss curves do not include any switching losses (turn-on and turn-off losses).

Maximum permissible case temperature

Fig. 4 and Fig. 7 depict maximum permissible case temperature for double side cooled arrangement as a function of average current for sine and rectangular waves respectively and for conduction angles ranging from 30° to 180° and DC. These curves have been derived for the maximum junction temperature of 125°C using the junction to case thermal resistances for the appropriate waveforms (see Table 9).

Maximum permissible heatsink temperature

Fig. 5 and Fig. 8 show the maximum permissible heatsink temperature for double side cooling, for sine and rectangular waves with conduction angles ranging from 30° to 180° and DC. These curves are calculated for the maximum junction temperature of 125°C and using the junction to heatsink thermal resistances for the given waveforms.

Thus from the curves of maximum power dissipation and maximum permissible case temperature, it is possible to calculate the required heatsink thermal resistance for a given ambient temperature.

Maximum (limit) transient thermal impedance – junction to case (°C/kW)

Fig. 9 gives the maximum transient thermal impedance curve, junction to case, for double side, anode side and cathode side cooling arrangements. Note that the unit is in °C/kW. The transient thermal impedance curve ($Z_{th(j-c)}$) gives the temperature response to a unit power step (1 kW). If the time interval is sufficiently long then the curve reaches the steady state DC value given in the table of Thermal and Mechanical Ratings. The $Z_{th(j-c)}$ curve is obtained by thermal modelling of the device using finite element (FE) method and is verified by measurements. An analytical equation of the curve is also given represented by the sum of four exponential terms:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{i=4} R_i \left(1 - e^{-t/\tau_i}\right)$$

The curve fit parameters R_i and τ_i are given in the table of Fig. 9. $Z_{th(j-c)}(t)$ is used to calculate the device junction temperature for time dependant power dissipation.

The two simplest and most common waveforms are the half sine and rectangular wave. With these repetitive wave shapes the peak junction temperature reached is slightly above that calculated using the average power dissipation and increases with decreasing conduction angle. To allow for this, incremental values ΔZ_{th} dependent upon wave shape are given in a table within Fig. 9. These values should be added to the values of appropriate $Z_{th(j-c)}(t)$ curve. Please note that ΔZ_{th} values are given in °C/W.

Multi-cycle surge current

Fig. 10 shows the surge current, I_{TSM}, as a function of the number of 10ms half sine wave pulses (50Hz) at T_{case} = 125°C and with no reverse voltage applied (V_R = 0 V). This curve is derived by calculating the value of the repetitive 50Hz current pulses that gives the same peak temperature as the rated single cycle surge current.

Single-cycle surge current

Fig. 11 shows the single-cycle, half-sine wave surge current capability, I_{TSM}, for varying pulse width. Also on the same graph the corresponding I^2t values are given. These variations are derived by calculating the current that gives the same peak junction temperature as the 10ms half-sine wave derived from the physical rating of the device. The test conditions are; T_{case} = 125°C and V_R = 0 V. Note that the device rating has been derated by 10% so that about 100 pulses can be tolerated over the life of the device.

Stored Charge

Fig. 12 gives the variation of stored charge (same as recovered charge) as a function of the rate of decay of on-state current (dI/dt). The measurement conditions are T_j = 125°C, $V_{R(peak)}$ = ~ 60% V_{DRM} and V_R = ~ 40% V_{DRM} with appropriate snubber to control the reverse voltage. The maximum and the minimum curves with model equations are given.

Reverse Recovery Current

In Fig. 13 the reverse recovery current associated with the stored charge of Fig. 12 is given. I_{RR} is also a function of junction temperature (see Fig. 26 in Appendix 6).

Gate Characteristics

Fig. 14 and Fig. 15 depict the gate characteristics. These are the graphs of gate voltage V_{GT} v the gate current I_{GT} with upper and lower limit curves.

In Fig. 14 the regions of uncertain triggering for -40°C, 25°C and 125°C are shown at the

left of the area defined by the upper and lower gate characteristic curves. Any areas on the right of the dividing lines are the preferred area of operation for each respective temperature. The upper limit curve gives the maximum values of V_{GT} and I_{GT} as appear in the table of Gate Characteristics and Ratings (e.g. V_{GT} = 1.5V and I_{GT} = 0.25A at T_j = 25°C for DCR3030V42). The embedded table in the Fig.14 gives the maximum permitted peak gate power dissipation P_{GM} (Watts) for various pulse widths and repetition rates.

For dynamic triggering, much higher peak gate current is recommended and Fig. 15 gives extended gate characteristics to include higher current and voltage range. Also on the graph are lines of constant peak power. These lines are the power limits corresponding to the values in the table embedded in the Fig. 14. For further details on thyristor gate triggering and characteristics please refer to Application Note AN4840.

PACKAGE DETAILS

The outline drawing of the package is given in the Fig. 16. Note that the same package type is used for devices with different voltage ratings. The particular device is highlighted in the table provided, which gives the maximum and minimum thickness appropriate to the device type.

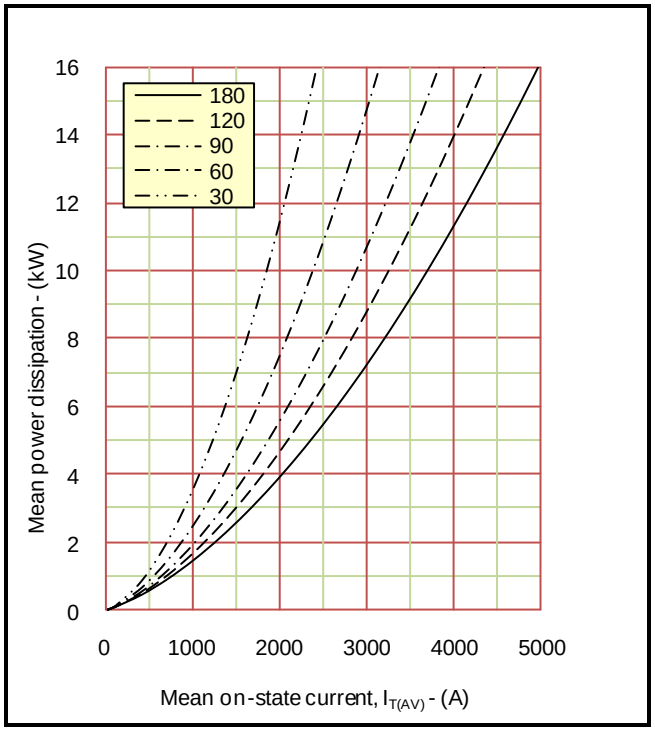


Fig.3 On-state power dissipation – sine wave

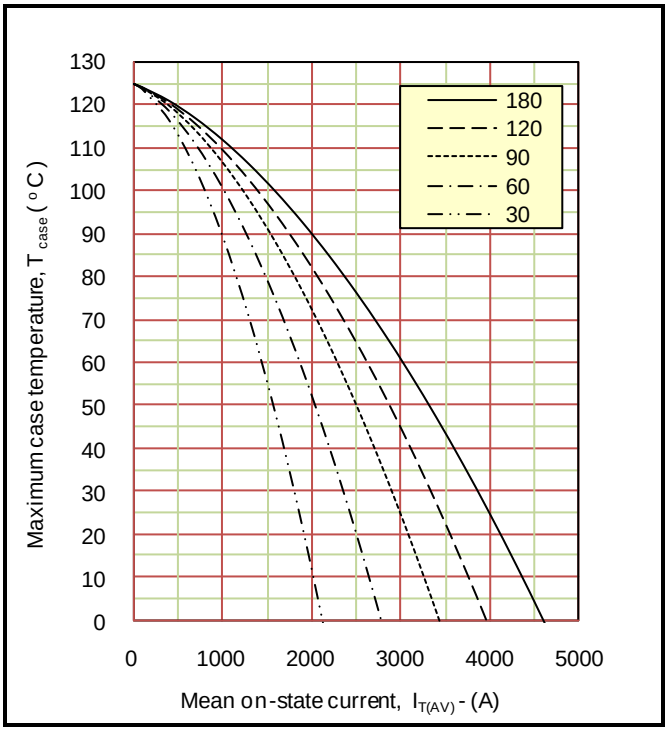


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

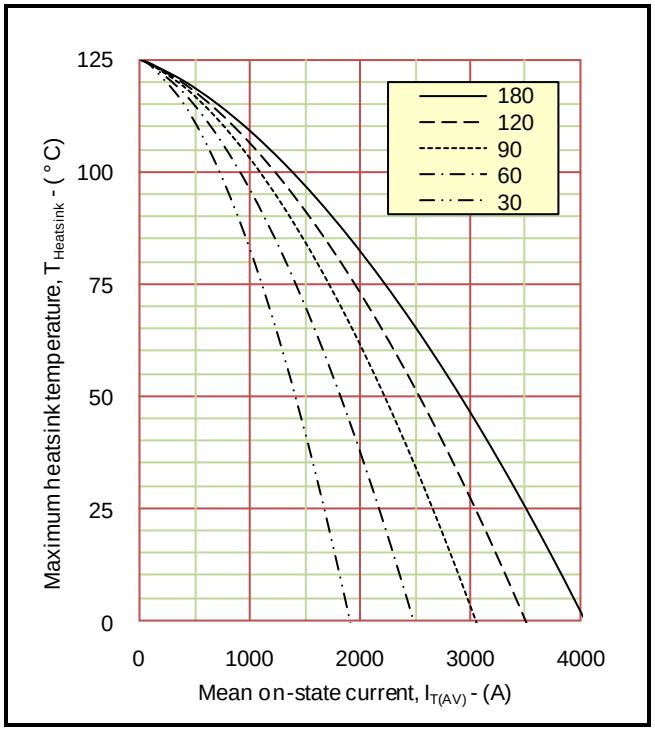


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

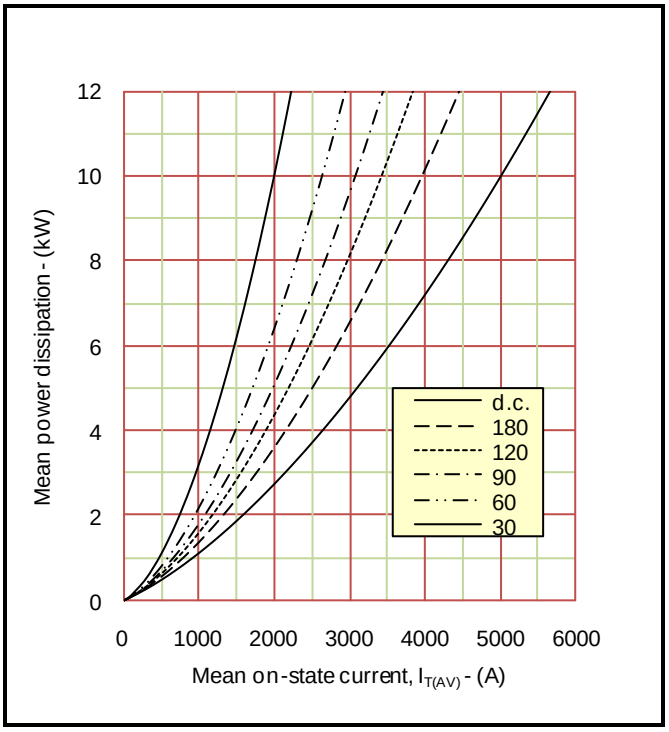


Fig.6 On-state power dissipation – rectangular wave

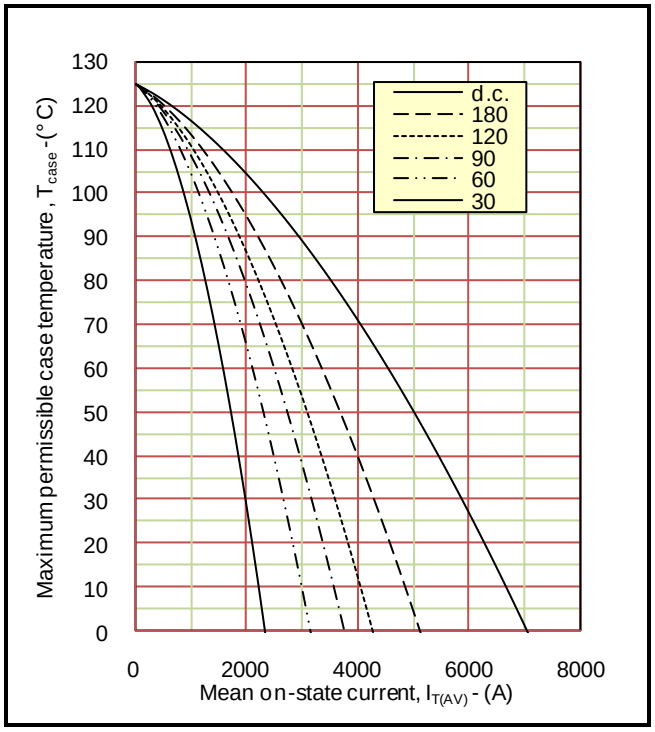


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

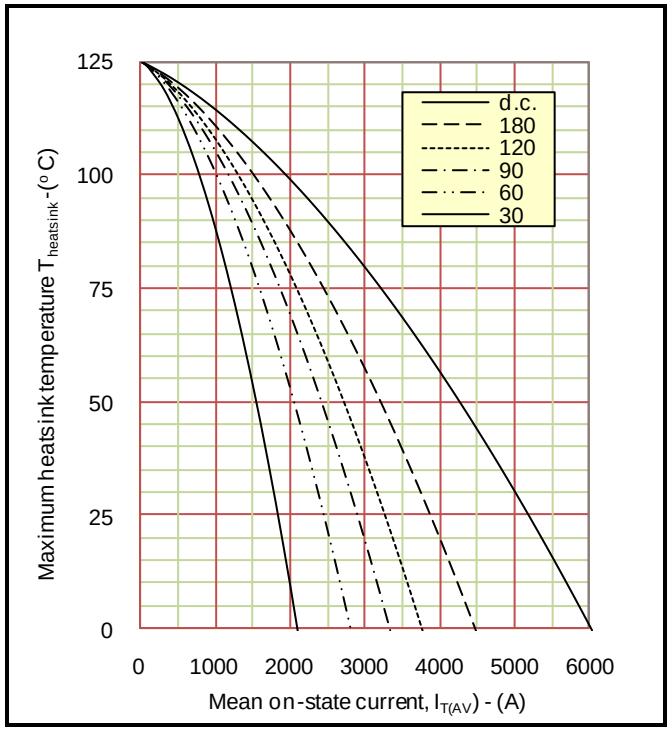
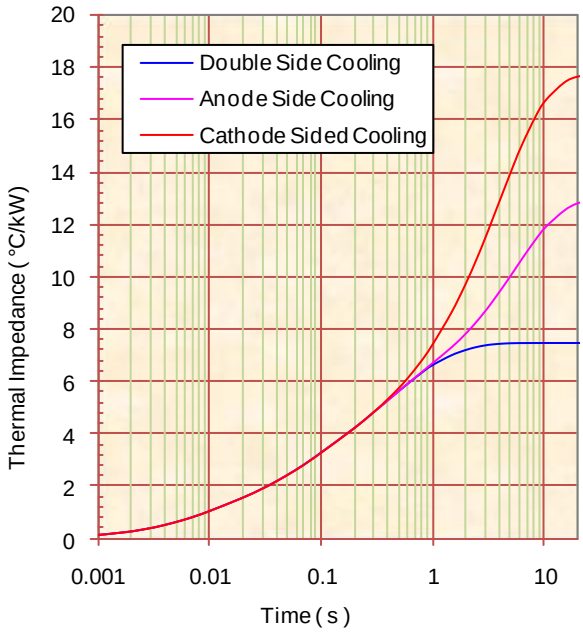


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R_i (°C/kW)	0.9206	1.8299	3.4022	1.3044
	T_i (s)	0.00768	0.05795	0.40786	1.2085
Anode side cooled	R_i (°C/kW)	0.9032	1.6719	3.0101	7.4269
	T_i (s)	0.00759	0.05365	0.31445	5.624
Cathode side cooled	R_i (°C/kW)	0.9478	2.0661	1.6884	13.0847
	T_i (s)	0.00784	0.06455	0.38944	4.1447

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T / T_i)]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)°C/W	
θ°	sine.	rect.
180	1.34	0.88
120	1.57	1.30
90	1.83	1.54
60	2.08	1.81
30	2.27	2.11
15	2.36	2.28

Anode Side Cooling		
	ΔZ_{th} (z)°C/w	
θ°	sine.	rect.
180	1.34	0.88
120	1.57	1.30
90	1.84	1.54
60	2.08	1.81
30	2.28	2.11
15	2.37	2.28

Cathode Sided Cooling		
	ΔZ_{th} (z)°C/W	
θ°	sine.	rect.
180	1.33	0.88
120	1.57	1.29
90	1.83	1.53
60	2.07	1.80
30	2.26	2.10
15	2.35	2.26

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

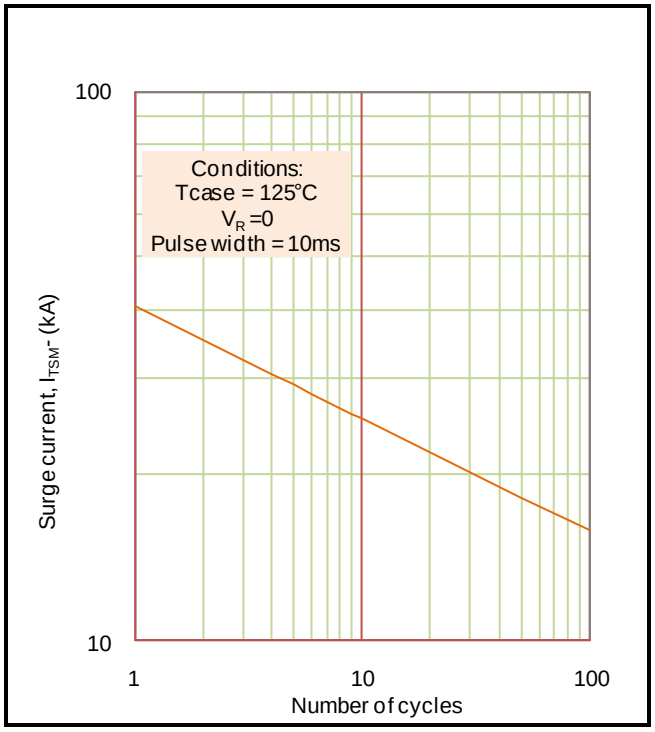


Fig.10 Multi-cycle surge current

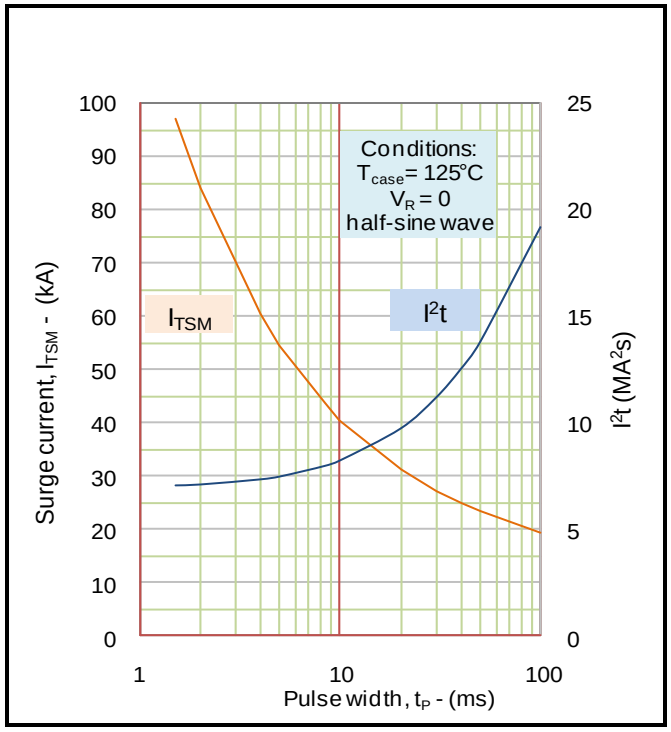


Fig.11 Single-cycle surge current

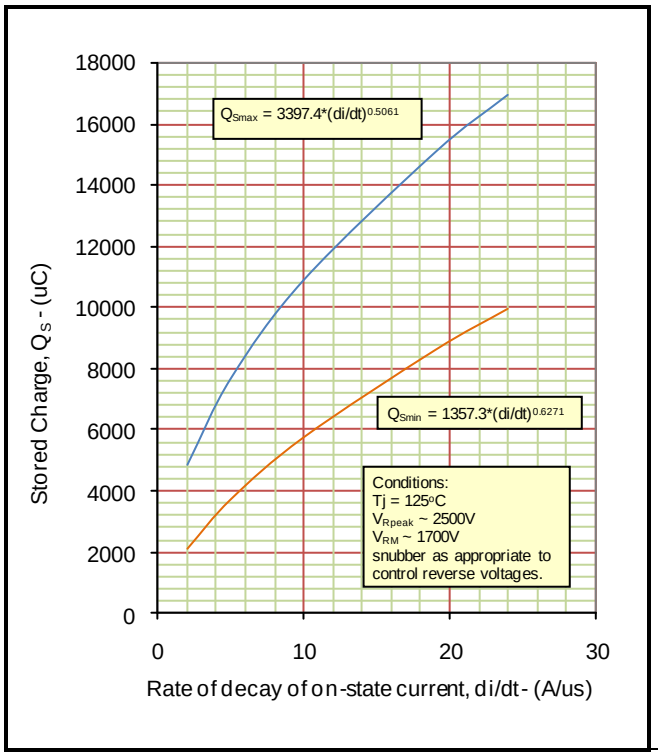


Fig. 12 Stored Charge

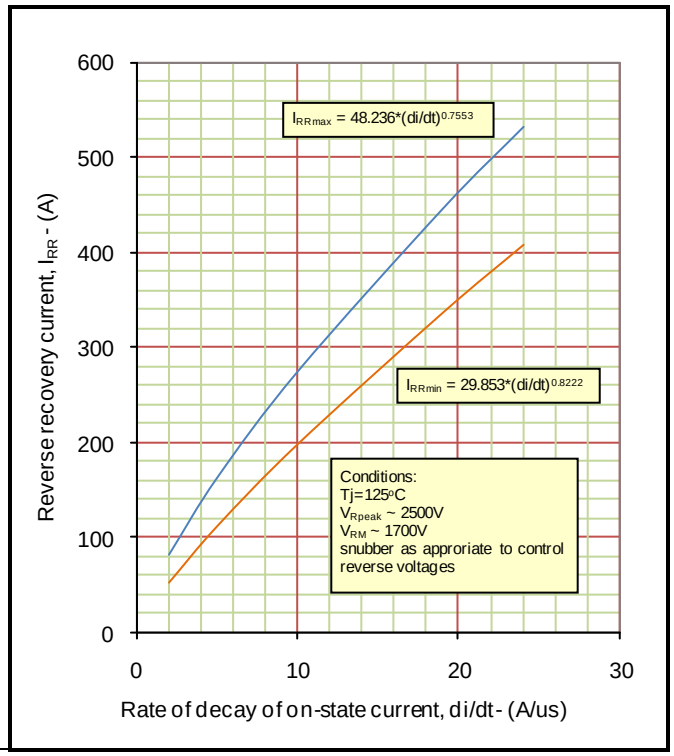


Fig. 13 Reverse Recovery Current

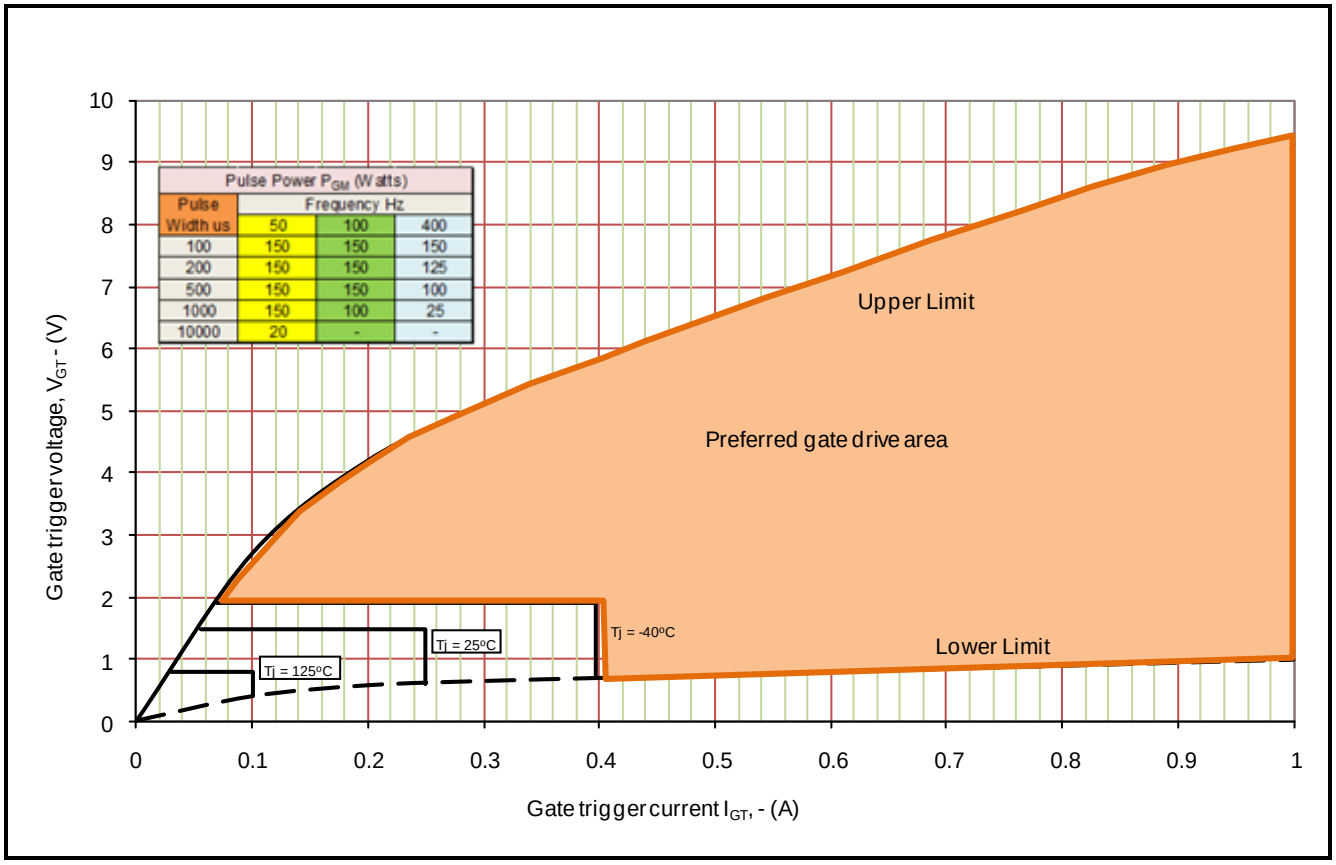


Fig14 Gate Characteristics

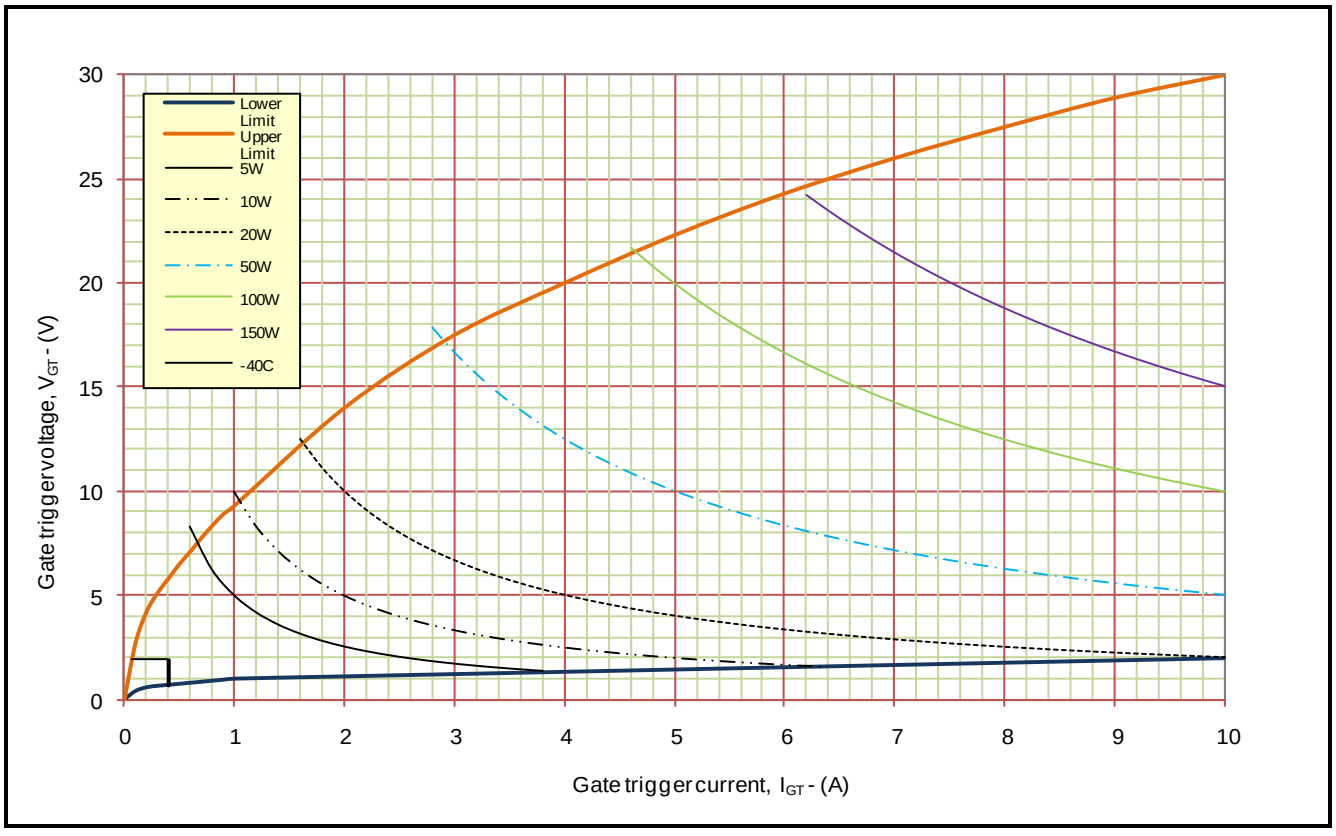
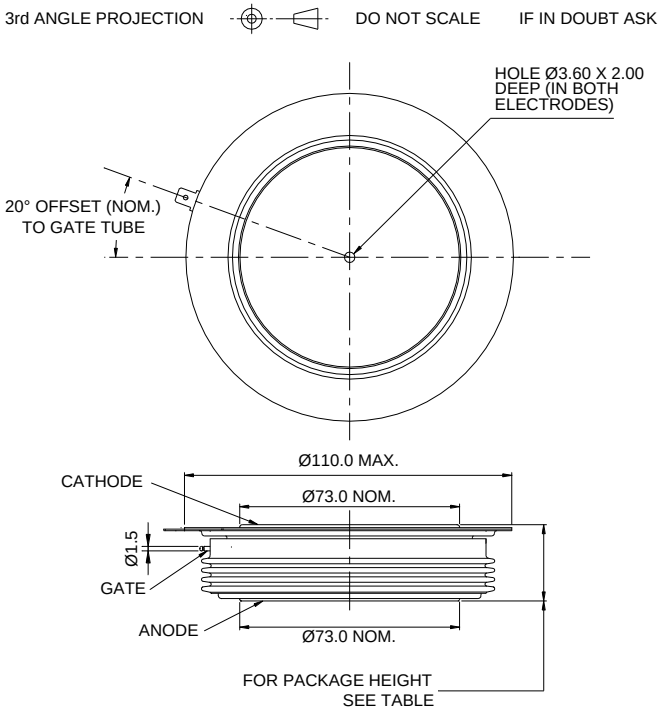


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR1474SV18	27.265	26.515
DCR1475SV28	27.34	26.59
DCR1476SV42	27.57	26.82
DCR1478SV48	27.69	26.94
DCR1574SV28	27.34	26.59
DCR1575SV42	27.57	26.82
DCR1576SV52	27.69	26.94
DCR4060V22	27.265	26.515
DCR3780V28	27.34	26.59
DCR3030V42	**27.57**	**26.82**
DCR2720V52	27.69	26.94
DCR2290V65	27.95	27.2
DCR1910V85	28.31	27.56

Lead length: 420mm

Lead terminal connector: M4 ring

Package outline type code: V

Fig.16Package outline

APPENDIX 1:

The Derivation of Average Current v Case Temperature Curves using the linear approximation to the Forward Volt Drop curve.

The Forward voltage drop curve of a thyristor can be approximated by the simple equation

$$V_{TM} = V_{T(TO)} + I \times r_T \quad (1)$$

where $V_{T(TO)}$ is the threshold voltage and r_T is the slope resistance (see Appendix 2).

The Power dissipated in the thyristor is given by :

$$P = I_{T(AV)} \times V_{T(TO)} + I_{RMS}^2 \times r_T \quad (2)$$

$$P = I_{T(AV)} \times V_{T(TO)} + k^2 \times I_{(AV)}^2 \times r_T \quad (3)$$

where k is the form factor of the waveform, $I_{T(AV)}$ is the average current and I_{RMS} is the RMS current.

The rise in junction temperature T_j above the case temperature T_{case} is given by

$$T_j - T_{case} = P \times R_{th(j-c)} \quad (4)$$

where $R_{th(j-c)}$ is the thermal resistance from junction to case corresponding to the form factor k.

Re-arranging this give

$$P = \frac{T_j - T_{case}}{R_{th(j-c)}} \quad (5)$$

Substituting this in equation (3) and re-arranging

$$(k^2 \times r_T) \times I_{T(AV)}^2 + V_{T(TO)} \times I_{T(AV)} - \frac{T_j - T_{case}}{R_{th(j-c)}} = 0 \quad (6)$$

Therefore, solving the quadratic equation (6) for $I_{T(AV)}$ we have

$$I_{T(AV)} = \frac{-V_{T(TO)} + \sqrt{V_{T(TO)}^2 - 4(k^2.r_T).(T_j - T_{case})/R_{th(j-c)}}}{2k^2.r_T} \quad (7)$$

Note that this is the average current rating ignoring any reverse recovery losses or turn-on losses that might need to be considered at higher frequencies or high di/dt at turn-on or turn-off. Also average current rating is referenced to the case temperature. Sometime the heatsink temperature (Fig. 17) is used for the reference temperature and in this case $R_{th(j-hs)}$ is used in the calculations.

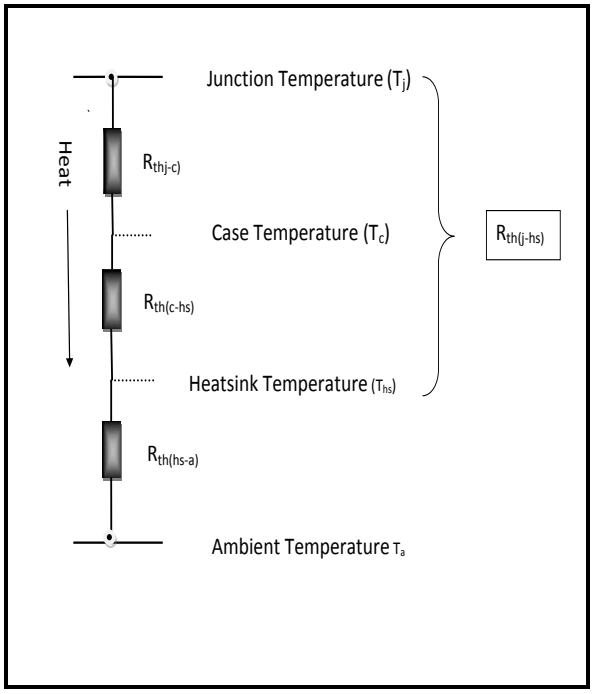


Fig.17 Thermal Circuit

APPENDIX 2:

Linear model of Thyristor on-state characteristics:

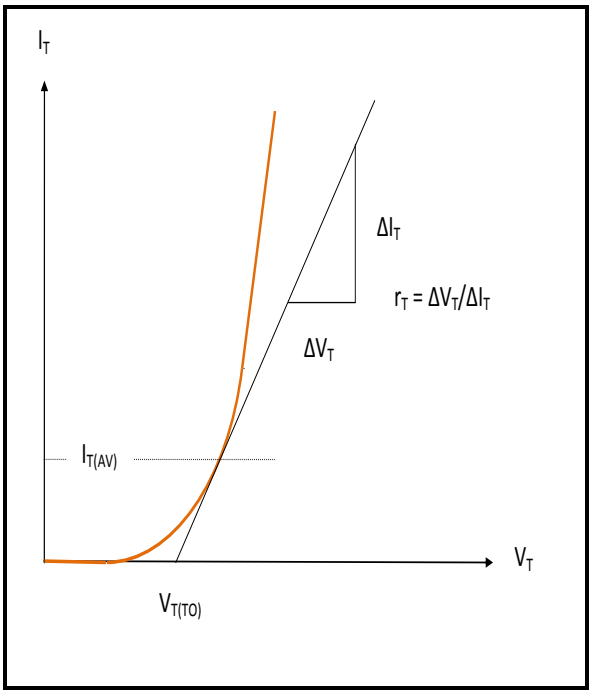


Fig.18 $V_{T(TO)}$ and r_T @ tangent to $I_{T(AV)}$

The linear approximation of the on-state characteristics of a thyristor is modelled by a straight line (piece-wise linear model) defined by an intercept on the x-axis $V_{T(TO)}$ (called the threshold voltage) and an inverse slope of the line r_T (called the slope resistance) as shown in the Fig. 18. The construction of the straight line leads to different definitions. Here are the four variations:

1. As illustrated in Fig. 18 where the line is tangent to the IV curve at the average current.
2. As shown in Fig. 19 where a chord is drawn through $I_{T(AV)}$ and $3xI_{T(AV)}$. The definition is commonly used for thyristors. For rectifier diodes a chord through $3I_{T(AV)}$ and $5xI_{T(AV)}$ sometimes gives a better result.
3. A variation of Fig. 19 which uses two straight lines instead of one to approximate to the true curve. In this version the lines pass through $1/6I_{T(AV)}$ and $\pi I_{T(AV)}$ and also $\pi I_{T(AV)}$and 20 x $I_{T(AV)}$.
4. As Fig 20. A tangential point constructed such that the value of $I_{T(AV)}$ calculated from $I_{T(AV)} = (-V_{T(TO)} \pm\sqrt{(V_{T(TO)}{}^2 + 4*k^2*r_T*P))/2*k^2*r_T}$ is the same as that calculated by more exacting methods. This method is a variation of method 1). It has been used to retrospectively calculate meaningful values of V_{T0} and r_T where more accurate current rating data already exists.

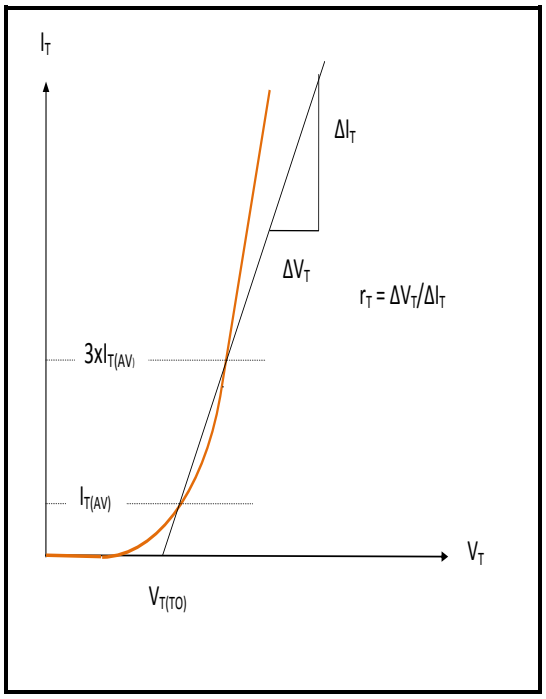


Fig. 19 $V_{T(TO)}$ and r_T represented by a chord

Dynex uses a variant of (3) with two straight lines; the first is a best fit straight line to the actual high current part of the forward voltage drop curve. A second line is then calculated for the best fit to the remaining low current part of the curve.

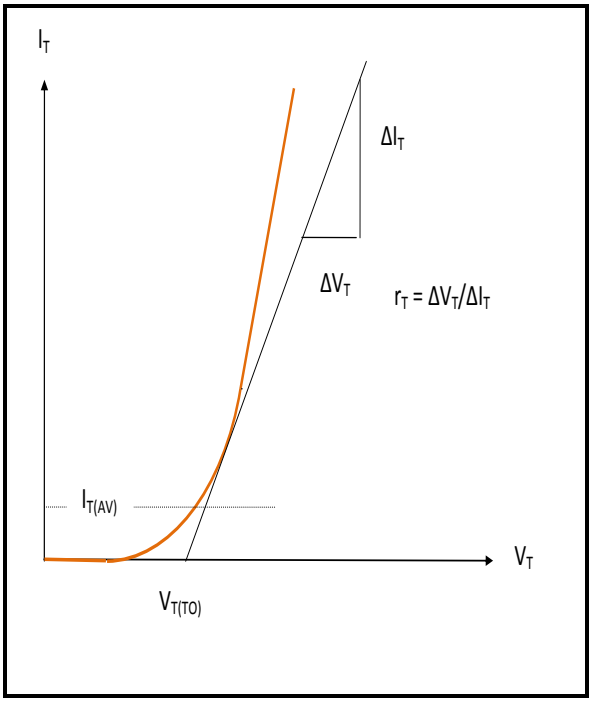


Fig. 20 Variation of tangent method

Limitations of $V_{T(TO)}$ and r_T model

Using any one of the first four models gives the correct value of the conduction losses at one or at most two points on the V_{TM} vs I_T curve, ie where the straight line meets the true curve. It can be seen that depending on where a point is taken on the curve the answers will be optimistic or pessimistic. Definitions 1, 2 and 4 give adequate accuracy up to 3 x $I_{T(AV)}$. The Dynex method gives reasonable accuracy at low currents and very good at the high current part of the curve and lesser accuracy in the intermediate region.

For improved accuracy a mathematical model is needed which approximates better to the true curve. This is the four coefficient curve for the equation given in the datasheet.

APPENDIX 3:

Clamping force requirements:

Fig. 21 shows the dependence of the thermal resistance $R_{th(j-c)}$ as a function of clamping force for a pressure contact thyristor. The minimum and the maximum values are chosen to be on the relatively flat portion of the curve. It is recommended to clamp the device using the value of the force between the minimum and maximum values quoted on the datasheets. Low value of clamping force results in increase in the thermal resistance and hence decreases in the device current carrying capability. Too high clamping force may reduce the device of thermal cycling capability and hence the product life.

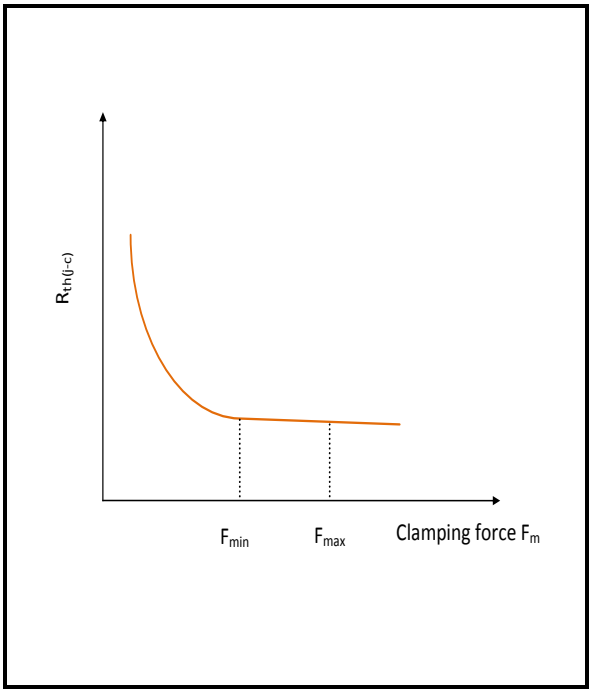


Fig. 21 Dependence of $R_{th(j-c)}$ on clamping force F_m

Please also refer to Application Note AN4839 for further details on clamping of power semiconductor devices.

APPENDIX 4:

Thyristor turn-on Characteristics

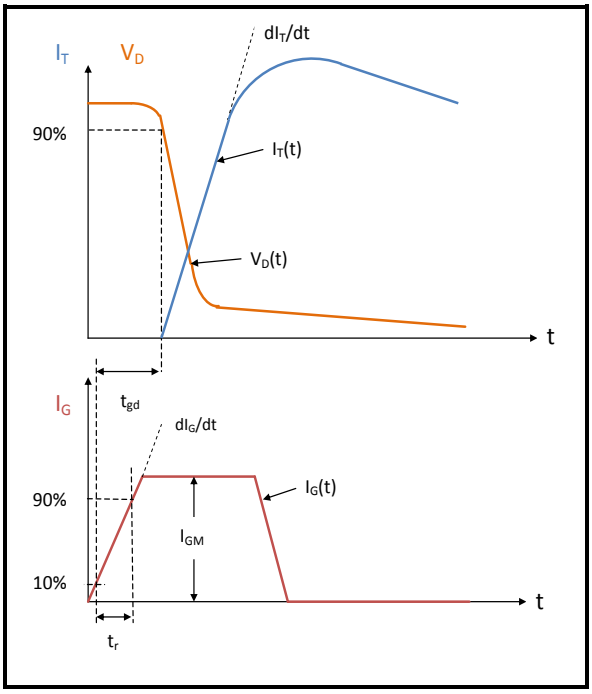


Fig. 22 Thyrisror turn-on waveforms

The turn-on process in a thyristor from its blocking state begins with the application of a gate signal. The thyristor current cannot flow instantaneously. A physical process called conductivity modulation takes place before the current is established in the thyristor. The time taken to undergo this process is called the turn-on delay time (t_d). This delay time is a function of gate signal (gate current amplitude I_{GM}, rise time of the gate current pulse t_r and the pulse-width of the gate current), the junction temperature T_j and off-state voltage V_d. For measurement purpose it is defined as the time interval between the gate current reaching 10% of its peak value and when the anode voltage drops to 90% of the applied forward blocking voltage V_D (see Fig. 22). On the datasheets it is called the gate controlled delay time t_{gd}.

APPENDIX 5:

Thyristor turn-off characteristics

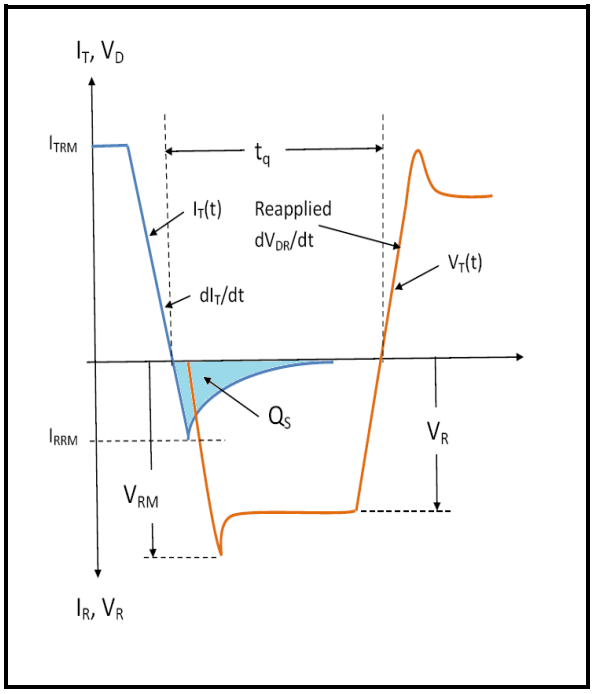


Fig. 23 Thyristor turn-off waveforms

Fig. 23 shows the schematic presentation of the turn-off waveforms for a thyristor and defines the dynamic parameters t_q and Q_S specified in the datasheets.

The turn-off process in a thyristor begins when the anode current falls below the holding current. However the thyristor cannot revert to the blocking state instantaneously because of the charge storage phenomenon. The stored charge in the thyristor has to be removed by carrier recombination and the reverse recovery process before a thyristor can resume the blocking state. The time taken to revert back to the blocking state is called the turn-off time (t_q). For measurement purpose it is defined as shown in Fig. 23. For a given switching application the off time should be longer than the t_q for a proper circuit function. Recovery charge Q_S

contributes towards the switching loss per pulse (see Application Note AN5951).

APPENDIX 6:

Dependence of T_q, Q_s, and I_{rr} on temperature and commutation conditions

The turn-off process in a thyristor begins when the anode current falls below the holding current. However the thyristor cannot revert to the blocking state instantaneously because of the stored charge phenomenon.

During conduction, current flow is achieved through the injection of excess carriers (charge) from the electrodes. As the forward current decreases towards extinction, a number of the excess carriers recombine at a rate governed by the carrier lifetime. It can be shown [1] that for fast rates of fall of the forward current (di/dt) the Stored Charge is dependent on the value of the forward current and independent of the di/dt and conversely, at slow values of di/dt the Stored Charge is independent of the forward current and dependent on the di/dt. The terms “fast” and “slow” are relative and are determined by the length of the current fall time relative to the carrier lifetime.

For most Phase Control Thyristor applications, the turn-off di/dt can be classed as “slow”, therefore the Stored Charge is independent of the initial current. Curves of the variation of Stored Charge and Reverse Recovery Current on di/dt are given in the data sheet at a Tvj of 125°C. Figure 24 shows the typical normalised dependence of Stored Charge on Tvj, while figure 25 is the corresponding curve for the Reverse Recovery Current.

Similarly [2] it can be shown that the time needed for the thyristor to regain the ability to block forward current (tq) is dependent upon temperature, di/dt and dV/dt. . Figures 26 to 28 show the typical, normalised dependence of tq on these conditions.

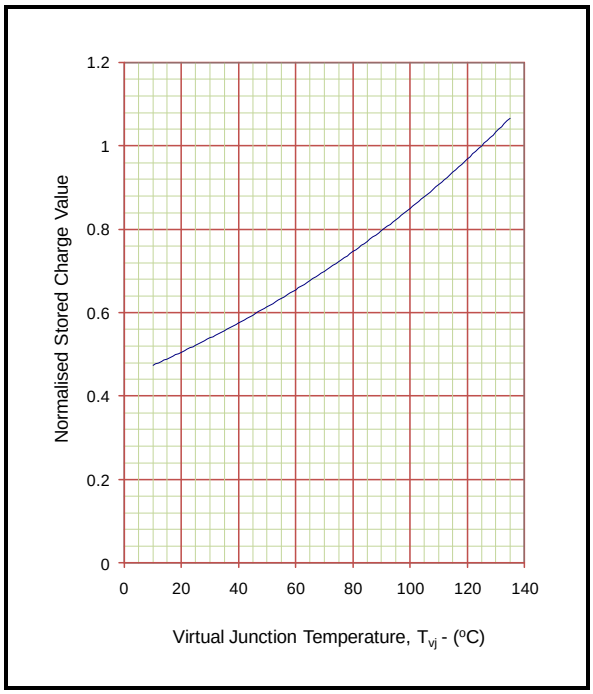


Fig. 24 Variation of stored charge with temperature

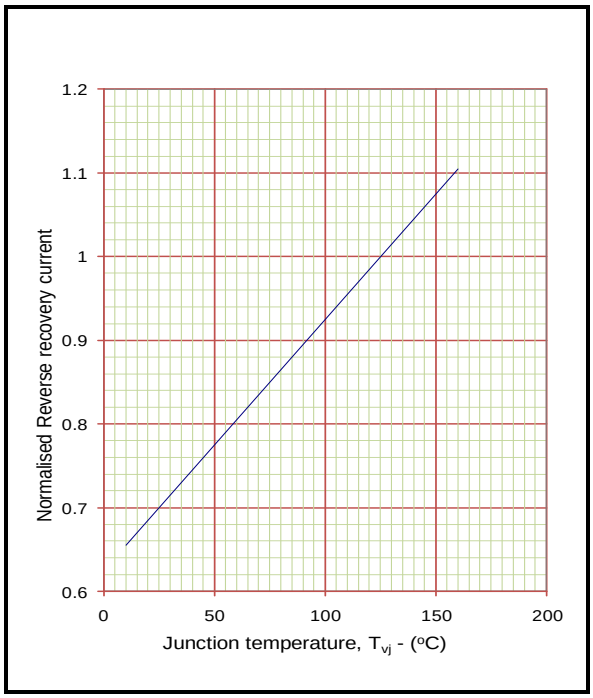


Fig.25 Dependence of reverse recovery current on junction temperature

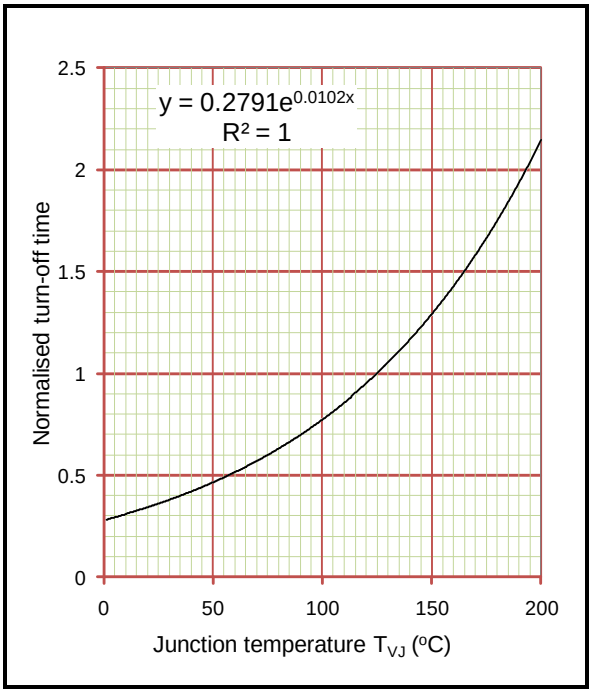


Fig. 26 Variation of t_q with temperature

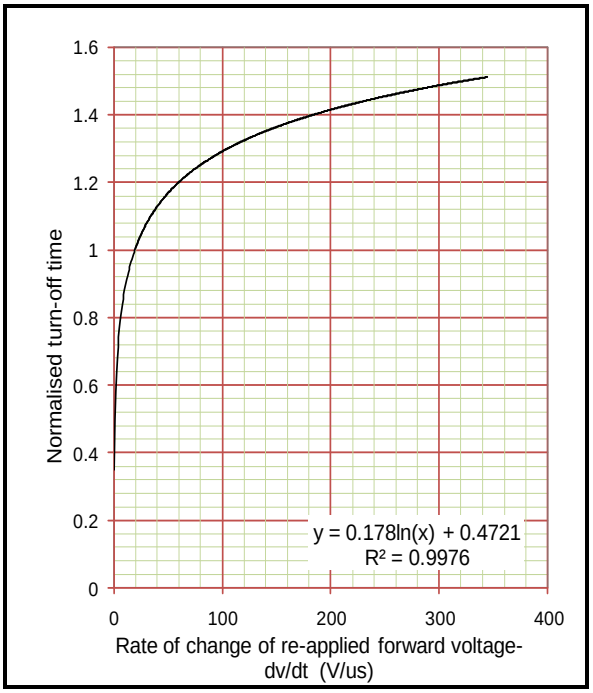


Fig. 28 Variation of t_q with dV/dt

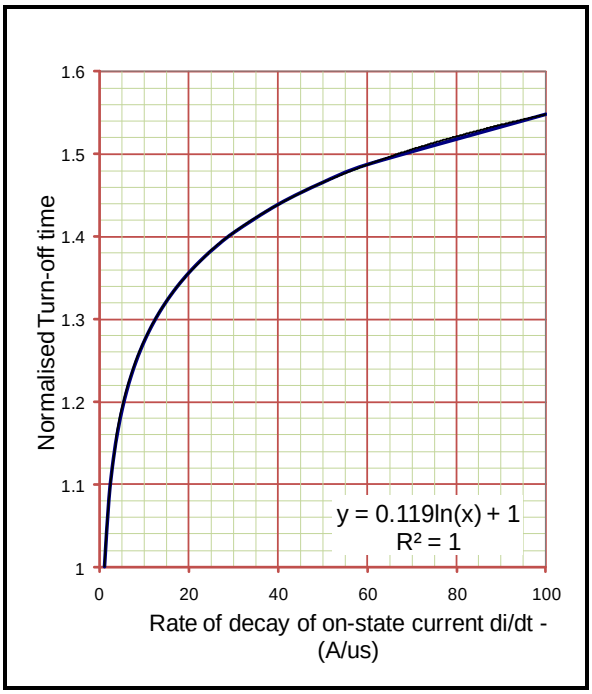


Fig. 27 Variation of t_q with dI/dt

References:

(1) P.D.Taylor (1987) '*Thyristor Design and Realization',*Wiley, England. P. 67

(2) Fukui, H., Naito, M., and Terasawa, Y. (1980). '*One dimensional analysis of reverse receovery and dV/dt triggering characteristics of a thyristor'*. IEEE Trans. Elelctron. Devices,**ED-27**, 596-602

HEADQUARTERS OPERATIONS

DYNEX SEMICONDUCTOR LIMITED

Doddington Road, Lincoln, Lincolnshire, LN6 3LF

United Kingdom.

Phone: +44 (0) 1522 500500

Fax: +44 (0) 1522 500550

Web: http://www.dynexsemi.com

CUSTOMER SERVICE

Phone: +(0) 1522 502753 / 502901

Fax: +(0) 1522 500020

e-mail: power_solutions@dynexsemi.com

PRODUCED IN UNITED KINGDOM