Email: powersolutions@dynexsemi.com
Main switchboard: +44 (0)1522 500 500
Website: www.dynexsemi.com

AN5381
Case Non-Rupture Current Ratings
Application Note

Replaces AN5381-1 AN5381-2 February 2014 (LN31349)

The non-repetitive surge current ITSM and the I^2t value define the limit of the electrical stress in the forward direction of a thyristor provided that it is triggered with sufficient gate current. These characteristics of the semiconductor are used to design short circuit protection, namely fuses or circuit breakers. By definition, this level of stress does not destroy the thyristors or diodes.

If a thyristor becomes short circuit in the forward direction and a current flows which is greater than the surge current limit, destruction of the encapsulation will not normally occur until this current is substantially greater than the surge current. This is because the thyristor is effectively triggered on by the fault current and normal injection over a large area of the silicon takes place.

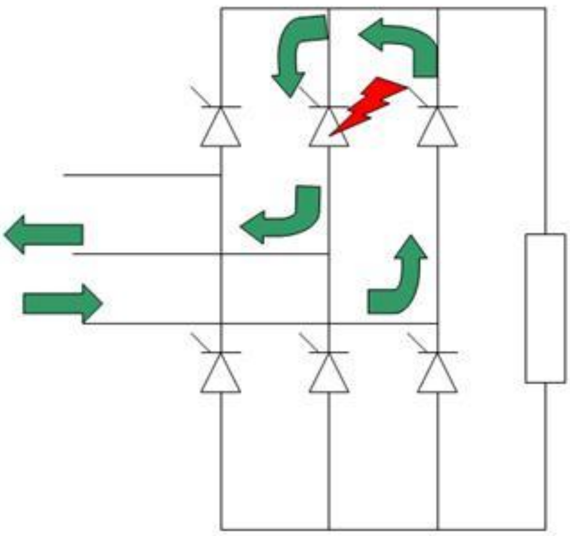

Fig 1. Fault current flowing back through a failed thyristor in a 3-phase bridge which shorts out two phases of the supply.

If the thyristor becomes defective in the reverse blocking state, a short circuit current can flow in the reverse direction. The cathode area that remains undamaged does not take part in carrying the current. A small edge around the failure melts and an arc develops in the case. The intense heat generated by the arc will lead to either cracking of the ceramic case through thermal shock or melting of the metal flanges of the encapsulation. Hot plasma then escapes through the breach into the enclosure. In high power installations where strong magnetic fields exist, an equipment short circuit or even burn down of the equipment may be the consequence.

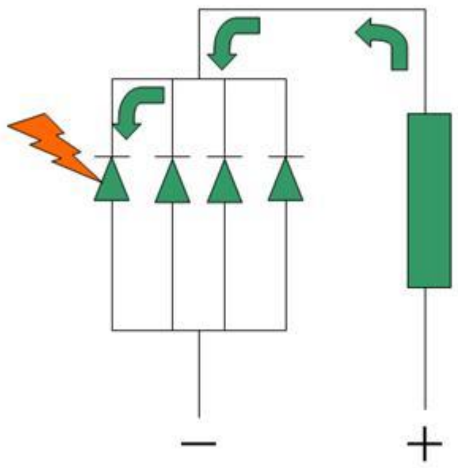

Fig 2. A failed device in a parallel application can experience a current equal to the full forward current through all parallel paths.

The case non-rupture current rating is the value of the half sine peak current, which can flow in the reverse direction through a failed device, that does not cause a mechanical failure of the encapsulation of the semiconductor, which remains hermetic.

Destructive tests in the reverse direction of thyristors show a large variation in the value of the non-rupture current depending on the location of the destroyed spot on the silicon pellet. The thick copper electrodes that contact the wafer restrain arcs at failure sites in the body of the silicon. Arcs at the edge of the silicon are the worst and produce the lowest values of case non-rupture current. Higher voltage devices in the same package as lower voltage devices have an inferior case rupture rating.

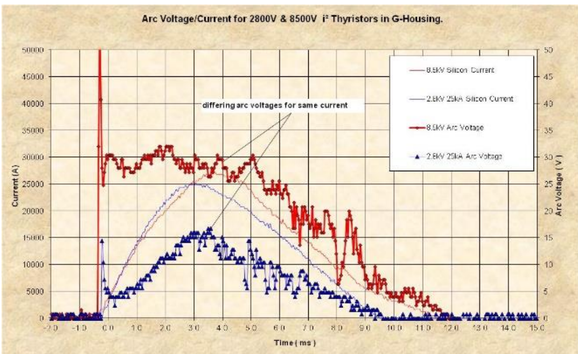

Figure 3. Reverse fault current and arc voltage

Figure 3, above, shows clearly that the arc power (I xV) is much higher for an 8.5kV device than 2.8kV device. Therefore the heat generated will be greater and case integrity will be lost at a lower current level.

For low voltage large diameter thyristors, the case non-rupture current is often smaller than the non-repetitive surge on-state current ITSM. Even for smaller devices, the use in parallel sets can cause problems.

For ease of measurement and also direct comparison with the surge current, case non-rupture currents are most commonly quoted for single half sine waves of 50Hz current. This is the IEC60747-6 test method and states that there will be no emissions from the device during the test, i.e. it will remain hermetic.

Using the values of case non-rupture current for 10ms half sine waves of current to calculate the peak current for other waveforms such as those in a circuit protected by a fuse is not recommended. The resulting answer is at best an approximation, at worst meaningless.
Devices should be tested with the actual fuse that it is proposed to use. The resulting peak case-rupture current will then also be dependent on the fuse characteristics but will be substantially greater than that for a 10ms half sine wave (see table).

Dynex Semiconductor Ltd. has conducted case non-rupture tests on some of its outlines of thyristor encapsulation. It has been found that it is the silicon thickness and resistivity, the ceramic design and the internal design of the encapsulation and ancillary components that determine the case non-rupture rating. Multiple tests of the same structure have given widely varying case rupture values even when the devices are forced to fail in the same physical location (see Description of test samples). Dynex has therefore concluded that it cannot design devices to have a specified value of non-case rupture rating and that it has no control of the variations that are observed. Any values of case non-rupture current are only indications of observed results to date and cannot be construed as ratings values or guarantees.

Testing devices has shown that there are three main places where the hermeticity of the device is breached.

At currents just above the rupture current the electric arc that is struck through the ionised gas inside the enclosure can burn through the thin copper of the flanges.

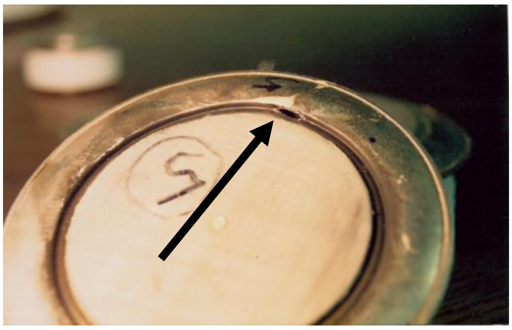

Fig 4. Thyristor after test showing hole burnt in copper flange

At higher current levels the ceramic can crack due to thermal shock.

Fig 5. Thyristor after test showing cracked ceramic due to thermal shock

Dynex has designed arc shields which contain the arc and keep it away from the ceramic and the flange.

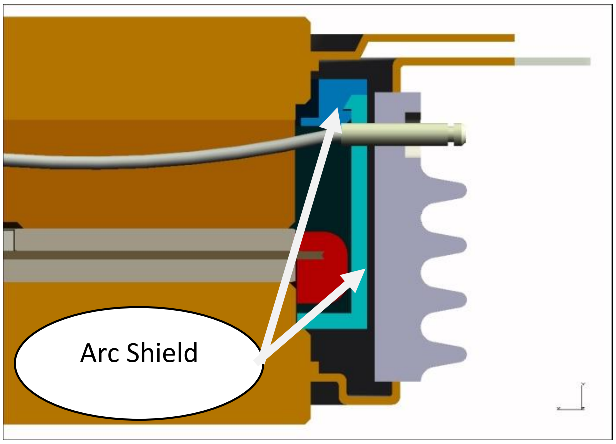

Fig 6. Schematic diagram of arc shield design

With the ceramic and flange shielded from the arc, the cold weld that joins the upper and lower flanges together is the weakest point and is pulled apart by the build up of pressure inside the ceramic. The resulting non case-rupture rating is substantially improved over that for devices without the arc shields. All these failure modes would emit hot ionised gas into an equipment cubicle.

Figure 7. Device with arc shield after test starting to swell due to internal pressure.

Figure 8. Device with arc shield after test at higher current than in Fig 7 with increased swelling due to internal pressure.

Fig. 8. Thyristor with arc shield finally failing at the cold weld due to internal pressure.

Illustrative non case rupture currents for a 75mm diameter, 2800V thyristor

Wave shape	Base width	Arc Shield ?	Peak current	I2t value
Half wave	10ms	No	34.8kA	$6MA^2s$
Half wave	10ms	Yes	77.5kA	$30MA^2s$
fused	6ms	Yes	120kA	$20MA^2s$

Basis of Tests

The test method was based on that described in IEC test method IEC60747 - 6. The test current source was a 50Hz generator and single phase transformer capable of delivering 500V RMS at up to 200kA peak. Varying the circuit voltage varied the test current. The circuit was capable of delivering discrete half cycles of current. All tests were conducted at room temperature.

Description of test samples

The basic units were specially prepared before assembly. As described above, the worst case condition is when the initial failure point is on the edge of the basic unit. A cut was made on the edge of each basic unit by air abrasion. At this stage the voltage blocking capability was still about 600V or 700V in both forward and reverse direction. This is too high to guarantee breakdown, so the fault was worsened by discharging a 16μF capacitor, charged to around 1000V, through each device. The reverse voltage was then seen to be degraded to below 200V. Only then were the basic units encapsulated in the ceramic housings. Again, to try and produce the worst case scenario, the failure point was aligned with the gate tube in the ceramic which might be deemed to be the weakest point.

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HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LIMITED
Doddington Road, Lincoln, Lincolnshire, LN6 3LF
United Kingdom.
Phone: +44 (0) 1522 500500
Fax: +44 (0) 1522 500550
Web: http://www.dynexsemi.com

CUSTOMER SERVICE
Phone: +44 (0) 1522 502753 / 502901
Fax: +44 (0) 1522 500020
e-mail: powersolutions@dynexsemi.com