



ACR2900VR45

Bypass Thyristor

Replaces DS6188-4 DS6188-5 June 2024 (LN43438)

FEATURES

- Double Side Cooling
- High Surge Capability
- Very Low Cosmic Ray FIT Rating
- High dV/dt Rating

APPLICATIONS

Multi-level VSC Bypass Thyristor for HVDC

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages VDRM and VRRM (V)	Conditions
ACR2900VR45	1000 / 4500	$T_{Vj} = -40$ °C to 125°C, IDRM = IRRM = 400mA,
		VDRM, VRRM tp = 10ms

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

ACR2900VR45

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

\mathbf{V}_{DRM}	1000V
\mathbf{V}_{DRM}	4500V
I _{T(AV)}	2920A
Ітѕм	39000A
dV/dt	10kV/µs
dl/dt	400A/μs

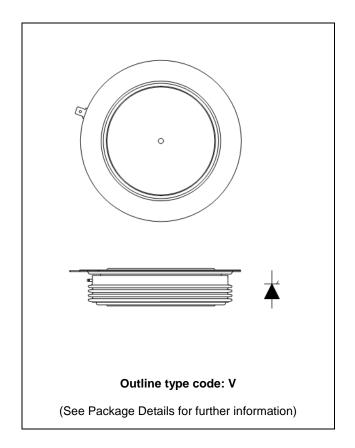


Fig. 1 Package outline

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CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Si	de Cooled			
IT(AV)	Mean on-state current	Half wave resistive load	2920	А
IT(RMS)	RMS value	-	4590	А
lτ	Continuous (direct) on-state current	-	4400	Α

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
Ітѕм	Surge (non-repetitive) on-state current	10ms half sine, T _{case} = 125°C	39.0	kA
l²t	I2t for fusing	V _R = 0	7.6	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
		Double side cooled	DC	-	7.5	°C/kW
Rth(j-c)	Thermal resistance - junction to case		Anode DC	-	13.0	°C/kW
	Single sid		Cathode DC	-	17.8	°C/kW
D	The second resistance and the best-industrial	Clamping force 54kN (with mounting compound)	Double side	-	2.0	°C/kW
Rth(c-h)	Thermal resistance - case to heatsink		Single side	-	4.0	°C/kW
Tvj	Virtual junction temperature	Blocking VDRM / VRRM		-	125	°C
Tstg	Storage temperature range			-55	125	°C
Fm	Clamping force			48	59	kN

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DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Test Conditions		Max.	Units
IRRM/IDRM	Peak reverse and off-state current	At VRRM/VDRM, Tcase = 125°C		-	400	mA
Vтм	Instantaneous forward voltage	At 5000A peak, Tj = 125°C		1.90	2.10	V
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 60°C, gate	open	-	10000	V/µs
dl/dt	Rate of rise of on-state current	From 67% VDRM to $2x I_{T(AV)}$ Gate source 30V, 10Ω $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$	Non-repetitive	,	400	A/µs
Veren	Threshold voltage - Low level	300A to 2600A at Tcase = 125°C			0.82	V
V т(то)	Threshold voltage - High level	2600A to 8000A at Tcase = 125°C		-	1.08	V
_	On-state slope resistance - Low level	300A to 2600A at Tcase = 125°C		-	0.30	mΩ
ľΤ	On-state slope resistance - High level	2600A to 8000A at Tcase = 125°C		-	0.20	mΩ
tgd	Delay time	$V_D = 67\% \ V_{DRM}, \ I_g = 3A$ $t_T = 0.5 \mu s, \ T_j = 25 ^{\circ}C, \ t_P = 40 \mu s$		-	3	μs
V pu	Pick-up Voltage $I_g = 3A$, $t_r = 0.5\mu s$, $T_j = 25$ °C, $t_p = 40\mu s$		-	2	V	
IL	atching current T _j = 25°C, V _D = 5V		-	3	Α	
Ін	Holding current	Тј = 25°С, Rg-к = ∞, Iтм = 500A, Iт = 5A		1	300	mA

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GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V GT	Gate trigger voltage	VDRM = 5V, Tcase = 25°C	1.5	V
V _{GD}	Gate non-trigger voltage	At 50% VDRM, Tcase = 125°C	0.4	V
lgт	Gate trigger current	VDRM = 5V, Tcase = 25°C	350	mA
IGD	Gate non-trigger current	At 50% VDRM, Tcase = 125°C	15	mA

CURVES

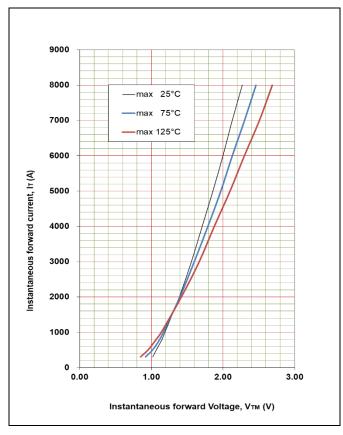


Fig. 2 Maximum on state characteristics

VTM EQUATION

 $V_{TM} = A + B.ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.232417

B = 0.081909

C = 0.000146

D = 0.006188

These values are valid for T_{j} = 125°C for I_{T} 300A to 8000A

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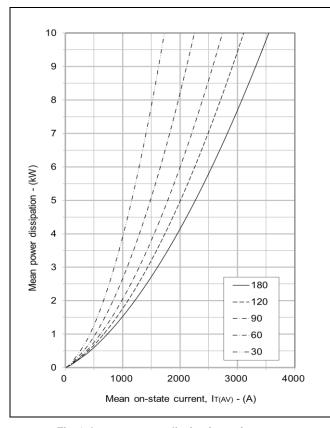


Fig. 3 On-state power dissipation - sine wave

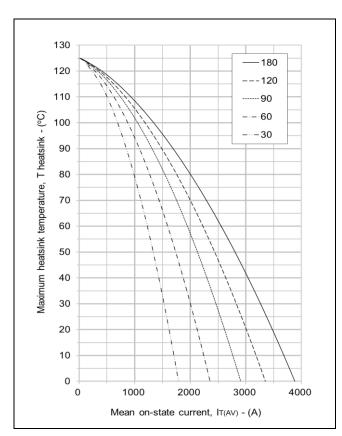


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

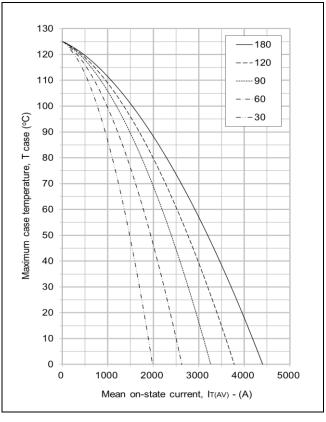


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

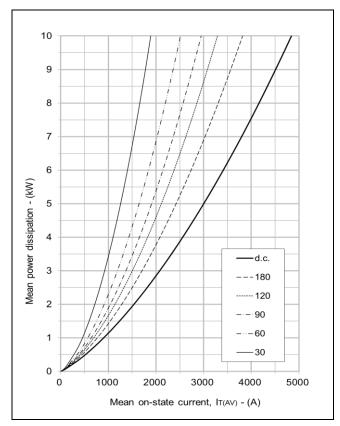


Fig. 6 On-state power dissipation - rectangular wave

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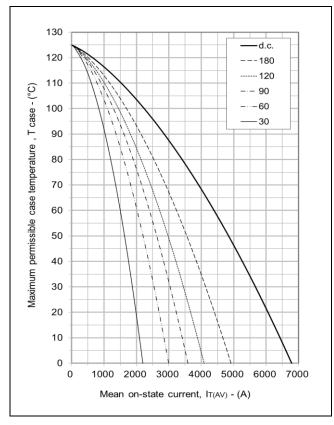
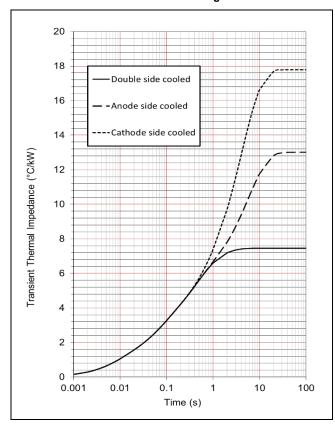


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave



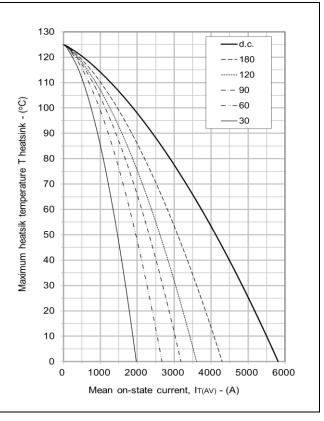


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

		1	2	3	4
Double side	Ri(°C/kW)	0.921	1.830	3.402	1.304
cooled	Ti(s)	0.008	0.058	0.408	1.209
Anode side	Ri(°C/kW)	0.903	1.672	3.010	7.427
cooled	Ti(s)	0.008	0.054	0.314	5.624
Cathode side	Ri(°C/kW)	0.948	2.066	1.688	13.085
cooled	Ti(s)	0.008	0.065	0.389	4.145

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

 $\Delta R_{\text{th(j-c)}}$ Conduction

Tables show the increments of thermal resistance R $_{\text{th}[j-c]}$ when the device operates at conduction angles other than d.c.

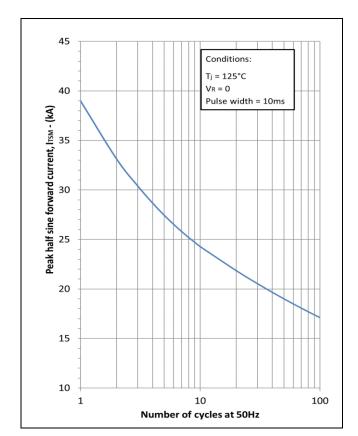
	Double side cooling			
	ΔZ_{th} ((z)		
θ°	sine.	rect.		
180	1.34	0.88		
120	1.57	1.30		
90	1.83	1.54		
60	2.08	1.81		
30	2.27	2.11		
15	2.36	2.28		

		anode Side Cooling			
		ΔZ_t	h (Z)		
	θ°	sin e.	rect.		
	180	1.34	0.88		
	120	1.57	1.30		
	90	1.84	1.54		
	60	2.08	1.81		
	30	2.28	2.11		
1	4.5	227	2.20		

Ca	thode Sided Cooling		
	ΔZ_d	_h (z)	
θ°	sine.	rect.	
180	1.33	0.88	
120	1.57	1.29	
90	1.83	1.53	
60	2.07	1.80	
30	2.26	2.10	
15	235	2 26	

Fig. 9 Maximum (limit) transient thermal impedance - junction to case (degC/kW)

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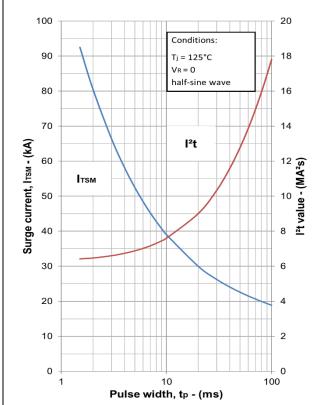


Fig. 10 Multi-cycle surge current

Fig. 11 Single-cycle surge current

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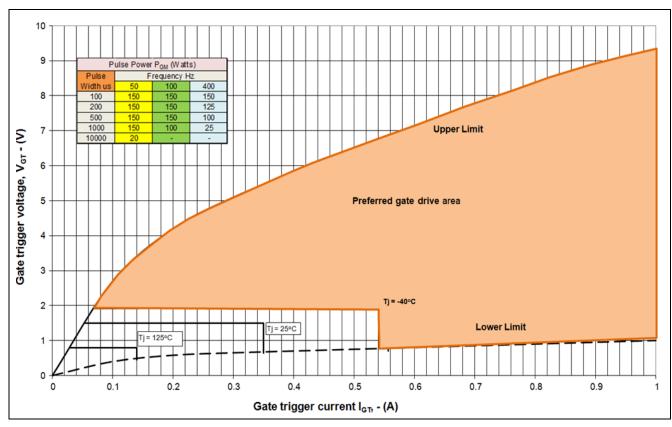


Fig. 12 Gate characteristics

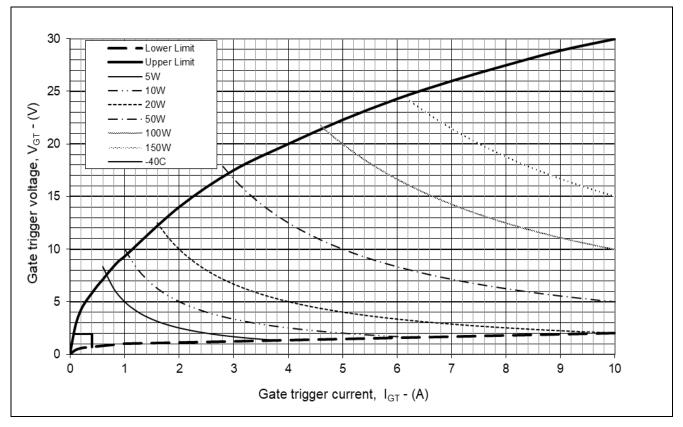


Fig. 13 Gate characteristics

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PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE

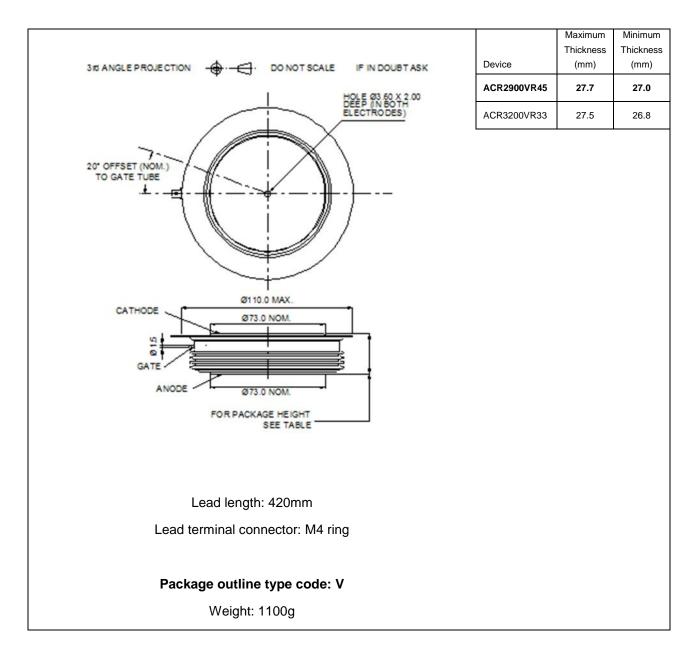


Fig. 14 Package outline

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