

AN6688

Power Semiconductor Module Lifetime Test, Modelling and Prediction

Application Note

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Abstract—This application note provides a guideline for lifetime test, modelling and prediction of power semiconductor modules used in power electronic systems under load conditions. The corresponding accelerated stress tests, underlying failure mechanisms and reliability diagrams are explained. It distinguishes between the rapid junction temperature swings of power cycling (PC) and the slower ambient-driven temperature cycling (TC). A framework is presented, to use PC and TC test diagrams along with the rainflow cycle counting algorithm for irregular stress extraction, and Miner's linear damage accumulation rule to predict lifetime. The goal is to provide all the necessary information for translating application requirements into a quantifiable reliability metric for power modules.

1 Introduction

The power electronic system is the heart of power generation, conversion, transmission and distribution application fields. The power semiconductor modules are the core component of these systems, and are subjected to a range of cyclic thermomechanical stresses during operation. These stresses are primarily caused by two distinct mechanisms: rapid, cyclic junction temperature variations—driven by converter switching losses and varying load currents, — and slow case temperature cycling driven by ambient conditions. Both mechanisms cause the power module's interconnection and soldering materials to expand and contract at different rates, resulting in thermomechanical fatigue and structural degradation, ultimately leading to module failure. The thermomechanical stresses induced by the load profile and ambient conditions must be restricted in accordance with the specifications in the power cycling (PC) and temperature cycling (TC) capability. Failure to:

- Accurately design the power electronics system,
- Select the appropriate power module, and
- Account for the thermal stresses

can lead to reduced operational lifetime for power module in field applications. Thus, a comprehensive understanding of power module

lifetime testing, modelling and prediction is vital for engineering robust and highly reliable power electronic systems. This application note systematically addresses this need and provides a structured framework for translating the thermal stresses experienced during field operation into a quantifiable lifetime prediction for power semiconductor modules.

The internal structure of the power module, fundamental failure mechanisms, and critical failure mechanisms are explained in Section 2. The accelerated stress tests for generating lifetime diagrams are described in Section 3. The step-by-step procedures are described in Section 4 for calculating the lifetime of a specific power module, because depending on different load profiles and varying thermal conditions, significantly different levels of thermomechanical stresses can occur even in applications using the same type of power module. The module lifetime estimation is performed by using lifetime diagrams, the rainflow cycle counting algorithm and Miner's damage accumulation rule, while considering the intended operational conditions.

For application-specific power module lifetime evaluation, Dynex can provide further analysis based on the relevant operating conditions and application requirements provided by the customer.

2 Failure mechanisms in Power module

Wire bonded power modules are a common package type widely used in industrial and transportation applications. As presented in **Figure 1**, a wire bonded IGBT module is made from different materials serving specific functions. The semiconductor chips are soldered onto a direct copper bonded (DCB) ceramic substrate. The top copper layer forms the electrical connections to the chips, while the bottom copper layer of the DCB serves as the connection to the module's baseplate, facilitating heat transfer to the cooling system. The ceramic layer between the copper sheets provides electrical insulation between the chips and the baseplate, while it transfers the heat from the chip to the baseplate. Aluminium (or Copper) bond wires are used for making interconnections between chips and chips to the substrate. The module assembly is completed with a baseplate, typically made of Cu or AlSiC,

acting as a heat sink. This baseplate plays a crucial role in transferring heat from the chip to the cooling system, ensuring effective dissipation of heat to maintain optimal operating temperatures.

Power module failure mechanisms are mainly classified into chip level failure and package level failure. Generally, electrical overstress may cause chip failure while package failure is usually caused by multiple factors and is related to the internal structure. Power module failures can be classified to three main categories, namely early failures, random failures and wear-out (long-term) failures.

Early failures are often attributed to defects introduced during the manufacturing process, material impurities, or design flaws. Unexpected overvoltage, overcurrent, system transients and system faults are main reasons for random failures, while thermal stresses coupled mechanical and environmental are the main causes for long-

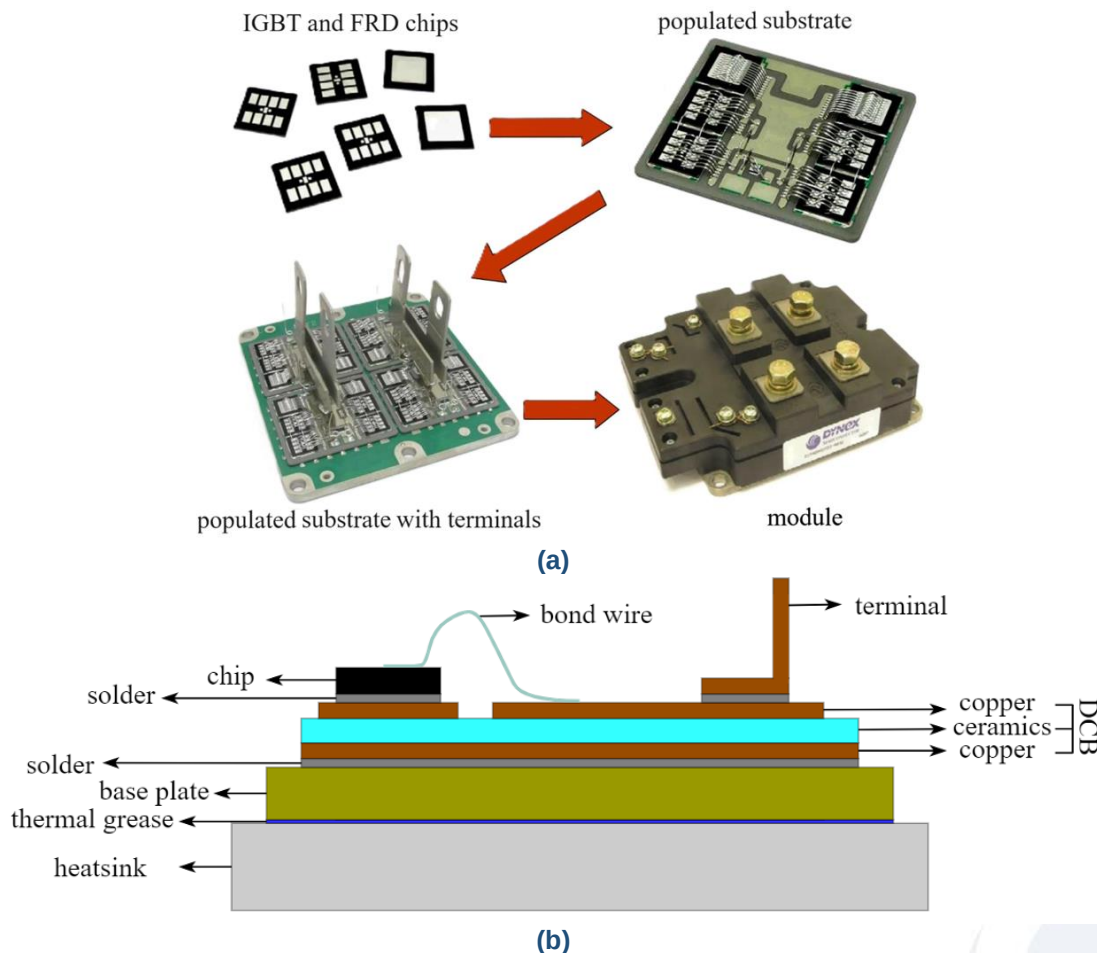


Figure 1. Wire bonded IGBT and fast recovery diode (FRD) module package. (a) A visual representation of the assembly process [1]. (b) A cross-sectional diagram of the module [2].

term failures. In this application note thermo-mechanical stress related long-term failures are considered for power module lifetime estimation. For further information on the failure mechanisms of IGBT power modules, refer to Dynex Application Note AN6442: IGBT Module Failure Mechanisms [2].

3 Power module reliability test

The reliability of wire bonds, die attach, substrate attach, busbar attach of standard power module consisting, is considered crucial for long term field application. Efforts have been made to improve the interconnection and attach technologies for power modules. The interconnection technologies have been advanced through the introduction of novel composition of Al or Cu wires, clips, ribbon bonding, as well as novel bonding technologies of bonding tool shape and bonding parameters. The improved attach processes of diffusion soldering and sintering have been implemented. The reliability of module is investigated using accelerated aging stress tests of power cycling (PC) and temperature cycling (TC). The experimental results are converted to PC and TC reliability diagrams and lifetime models.

3.1 Power cycling (PC)

The ultrasonic wire bonding process is used for the electrical interconnection of semiconductor chips and chips to DBC substrate. A typical IGBT power module is shown in **Figures 2**, which has approximately 360 wires and 1050 wedge bonds.

The reliability of chip-near interconnects i.e., bond wires and the solder below the chip is assessed through PC test.

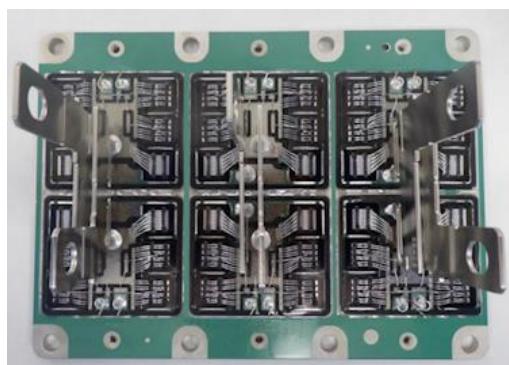


Figure 2. Internal view of an IGBT module

In the test, the chips are heated by applying a constant load current until the maximum junction temperature (T_{jmax}) is reached. The current is then switched off, and the chips are cooled until the T_j approaches the case temperature T_c , which is approximately equal to the temperature of the cooler mounted on the baseplate. The same test conditions are periodically repeated during each cycle, and the cycle including heating and cooling lasts for several seconds. The temperature variation in PC test is shown in **Figure 3**.

The repetitive and rapid T_j variations during PC testing induce cyclic stress at the bond interface, driven by the mismatch in the coefficient of thermal expansion (CTE) between the bond wire and the chip top-side metallisation. This repeated stress causes micro-cracks to initiate and propagate at the interface between the bond wire and the chip metallisation. This process eventually leads to immediate plastic deformation and the complete detachment of the wire—a failure mode known as bond wire lift-off. In addition to stress at the bond interface, bending stress is concentrated at the heel of the bond wire, where cyclic contraction and expansion lead to crack initiation and propagation, ultimately causing the wire to fracture.

Beyond bond wire degradation, the chip top-side metallisation itself undergoes cyclic compressive and tensile stresses due to the CTE mismatch with the underlying silicon. These stresses cause a redistribution of aluminium grains, resulting in surface roughening and extrusion of aluminium. This metallisation reconstruction increases the sheet resistance of the metallisation, contributing to a rise in on-state voltage. Furthermore, it weakens the surface to

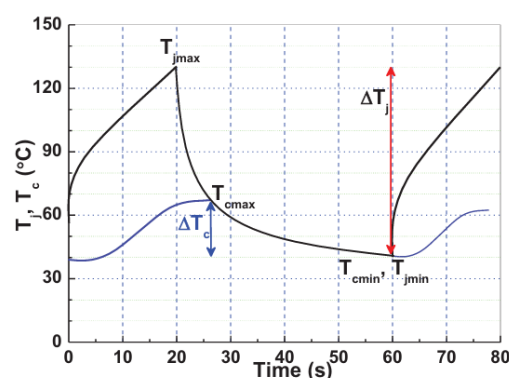


Figure 3. The temperature profiles in PC test [3].

which the bond wires are attached, thereby accelerating bond wire lift-off. The failure modes observed during PC testing are located on chip-near-interfaces and include bond wire lift-off, bond wire heel cracks, die-attach solder delamination, and aluminium reconstruction on the chip top surface as shown in **Figure 4**. The failure criterion is defined as either increase of on-state voltage by 5% or an increase of thermal resistance R_{th} by 20% from its pre-test value.

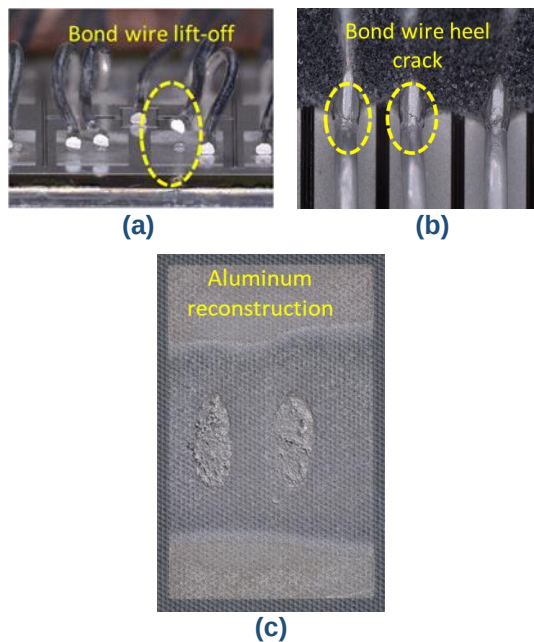


Figure 4. Bond wire and chip bond pad degradation due to thermomechanical fatigue. (a) Bond wire lift-off. (b) Bond wire heel cracks. (c) Chip top aluminium metal reconstruction.

As an example, the PC result diagram of IGBT power module DIM1500ASM45-RT501 is shown in **Figure 5**. It shows the number of cycles completed at failure (N_f) under a single test condition e.g., $N_f = f(\Delta T_j)$ with T_{jmax} kept constant during each PC cycle; ΔT_j is difference between minimum and maximum T_j during the PC test. In this figure, the solid lines show the experimentally validated N_f obtained from laboratory accelerated PC tests, whereas the dotted lines represent an estimated N_f based on modelling. The PC lifetime curves represent a defined probability that 10% of modules in a population are expected to reach end-of-life criteria by given number of N_f cycles.

The PC tests are performed with varying heating time t_{on} 1-3s, while $t_{cycle} = t_{on} + t_{off}$ varies depending on the device type and the required ΔT_j .

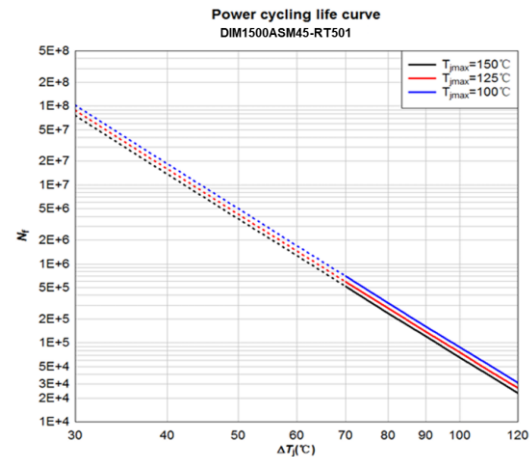


Figure 5. Number of cycles to failure (N_f) vs ΔT_j during PC at fixed $t_{on}=3s$ for constant T_{jmax} of 100°C, 125°C and 150°C

The t_{on} has impact on the module lifetime. Hence, the PC capability dependency on t_{on} time is provided. **Figure 6** shows the t_{on} dependency of Dynex IGBT5 A-outline industrial modules for t_{on} ranging from 0.1s to 60s, with PC test at fixed $t_{on} = 3s$ serving as a reference. The derating factor i.e., normalized N_{cycle} for different t_{on} , given in **Figure 6**, should be applied to N_f calculations from **Figure 5**. To approximate, the limits of 0.1 can be used for $t_{on} < 0.1s$ and 60 can also be used for $t_{on} > 60s$.

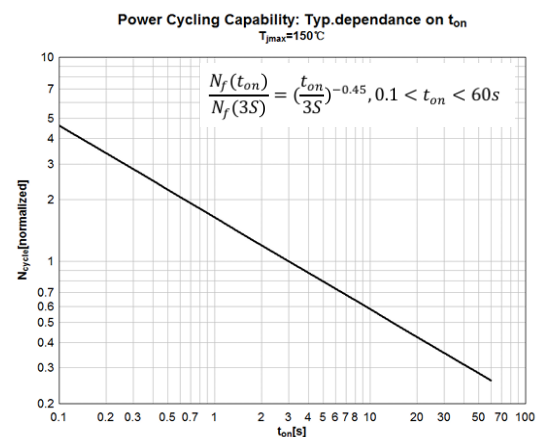


Figure 6. The dependency of N_f on t_{on} during PC test for Dynex IGBT5 A-outline industrial modules.

3.1.1 Example

An example of PC lifetime prediction of DIM1500ASM45-RT501 is described as follows. In the application, the IGBT has power on

time of 5s in a 35s cycle, and T_j rises from 80°C to 125°C i.e., $\Delta T_j = 45^\circ\text{C}$.

According to the PC diagram of **Figure 5**, the N_f is 8×10^6 cycles for $\Delta T_j = 45^\circ\text{C}$ and $t_{on} = 3\text{s}$. For $t_{on} = 5\text{s}$ a derating factor of 0.8 from **Figure 6** should be applied, meaning the PC lifetime is $N_f = 6.4 \times 10^6$ cycles.

A further example of PC lifetime prediction for a more complex load profile in a traction application is presented in Section 4.

3.2 Temperature cycling (TC)

Accelerated passive TC test is a typical and effective way to evaluate the substrate attach and busbar attach solder degradation due to thermal stresses.

In a TC test, the power module is mounted on a copper plate for heating and cooling. The module undergoes repeated transitions between high and low case temperature (T_c) without electrical power applied. For a typical passive TC strategy, the T_c varies from 45°C to 125°C with an error of $\pm 5^\circ\text{C}$ and the cycling period is in several minutes. The relatively long intervals of T_c fluctuations degrade the solder layer between substrate and baseplate and solder attaching busbar to substrate. **Figure 7** shows the T_c variation during the TC test.

Due to different in CTE of materials and temperature gradient experienced by each layer, time dependent creep and irreversible plastic deformation occurs and contributes to delami

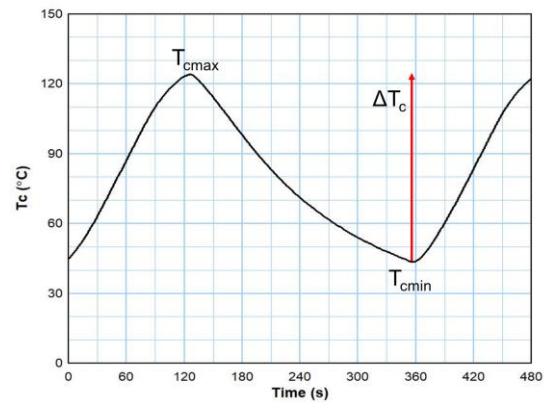


Figure 7. Case temperature (T_c) profile in TC test.

nation and cracks initiating and penetrating from the corner to the centre of substrate solder layer. The failure modes during passive TC are delamination on the edges of substrate attach solder and cracks in the solder jointing busbar and substrate [4]. The failure criteria for TC test is increase of R_{th} by 20% from its pre-test value.

Figure 8 shows the scanning acoustic microscopy (SAM) images illustrating the impact of different baseplate materials on substrate attach solder degradation during various TC tests. The copper is well known for easy mechanical handling and high thermal conductivity. However, CTE mismatch between copper and ceramic substrate is high, which will create substrate attach solder cracks during heavy load cycles and resulting in high thermal impedance between chips and baseplate. AlSiC baseplate modules are typically used in railway traction converters, wind turbines and high-reliability industrial

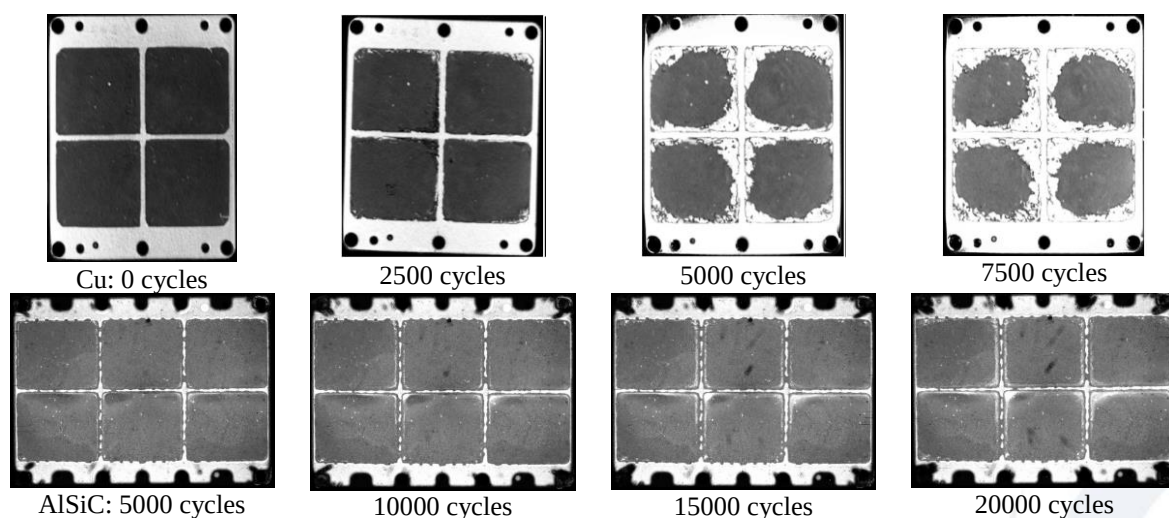


Figure 8. SAM images of IGBT module substrate attach solder under various TC cycles with Cu and AlSiC baseplate.

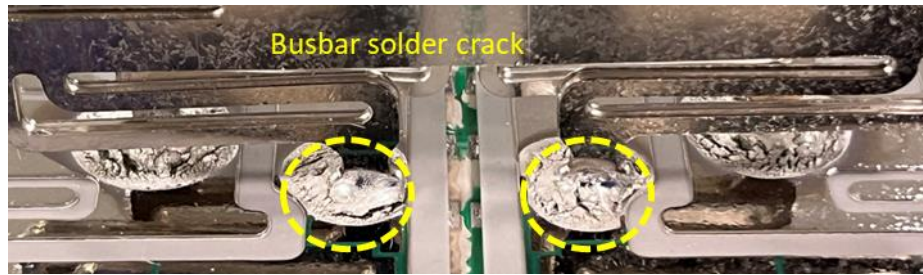


Figure 9. Optical images of cracks in busbar solder due to TC.

applications where a long service life under repeated TC is essential. The AlSiC is relatively stiff materials and have low CTE mismatch with ceramic substrate. This results in high TC reliability and delayed solder delamination compared to Cu baseplate. Figure 9 shows the cracks in the busbar-to-substrate attach solder during TC.

The TC test lifetime diagrams of DIM1500ASM45-RT501 IGBT modules (with an AlSiC baseplate) and the DIM900M1HS12-PG500 IGBT module (with Cu baseplate) are shown in Figure 10 and Figure 11, respectively. It shows $N_f \cong f(\Delta T_c)$, with either T_{cmin} or T_{cmax} kept constant during TC test. The heating up and cooling down times in a TC cycle are typically 2 minutes each. In Figure 10, the solid line shows the experimentally validated N_f obtained from laboratory accelerated TC tests, whereas the dotted line represent an estimated N_f based on modelling. The TC lifetime curves represent a defined probability that 10% of modules in a population are expected to reached end-of-life criteria by given number of N_f cycles.

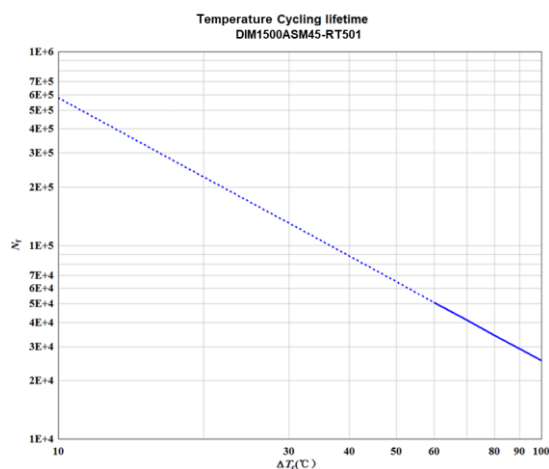


Figure 10. N_f vs ΔT_c during TC test with $t_{on}=t_{off}=2\text{min}$ and constant T_{cmin} of 25°C for power module with AlSiC baseplate.

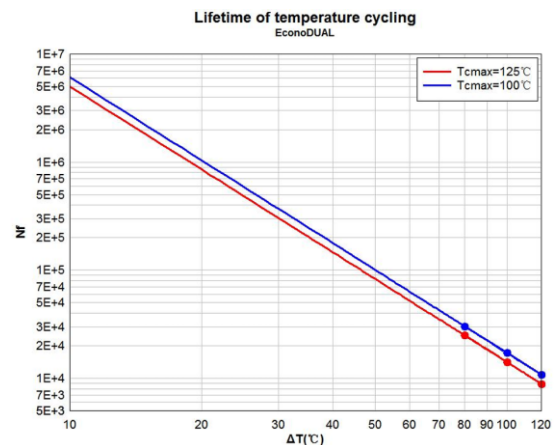


Figure 11. N_f vs ΔT_c during TC test with $t_{on}=t_{off}=2\text{min}$ and constant T_{cmax} of 100°C and 125°C for power module with Cu baseplate.

4 Lifetime prediction

To estimate the expected service lifetime of a power module in application, it is required to sum up the number of cycles within the scope of T_j/T_c mission profile. After this, the damage associated with each cycle is evaluated using the appropriate PC/TC lifetime diagram. The rainflow counting algorithm and Miner's damage accumulation rules are most widely used methods in this analysis.

4.1 Rainflow counting algorithm

For load cycles with a complex, varying temperature profile, the rainflow stress cycle counting algorithm is used to reduce the spectrum of varying stress into a set of simple cycle numbers.

The temperature-time in mission profile is rotated 90 degrees clockwise, so time points downward. The curve now looks like a series of pagoda roofs. The rules of rainflow counting are based on water flowing down these roofs [5]. A flow of "rain" begins at the inside of each peak (local maximum) and valley (local

minimum). The flow stops when one of these conditions is met:

- It reaches a point on the "roof" opposite an equal or more extreme peak or valley than its starting point. (e.g., flow from a peak stops when it reaches a point opposite an equal or higher peak than the starting point, likewise flow from a valley stops when it reaches a point opposite an equal or lower valley than the starting point).
- It merges with the flow from a previous roof.
- It reaches the end of the time history.

When a flow stops, a half cycle is counted. The half cycle's ΔT and mean are determined by the starting point and the termination point of flow [6].

4.1.1 Example

An analytical mission profile of T_c is shown in **Figure 12**, and it's analysed by rainflow approach.

- Drop A starts from a valley and terminate at a valley which is equal to the valley of starting point.
- Drop B starts from a peak and terminates when it passes a peak which is higher than peak of starting point.
- Drop C merges with run of drop A.
- Drop D merges with drop of F.
- Drop E starts from a valley and terminate at a valley which is equal to the valley of starting point.
- Drop F falls out because of reaching the time history.

There are following half cycles of ΔT stress in this mission profile:

- $N_1 = 2 \times \Delta T = 70^\circ\text{C}$; 1 complete cycle
- $N_2 = 2 \times \Delta T = 20^\circ\text{C}$; 1 complete cycle
- $N_3 = 2 \times \Delta T = 35^\circ\text{C}$; 1 complete cycle

With the information of cycle numbers in T_j/T_c mission profile, the stress lifetime can be calculated from lifetime diagrams and Miner's damage accumulation rule .

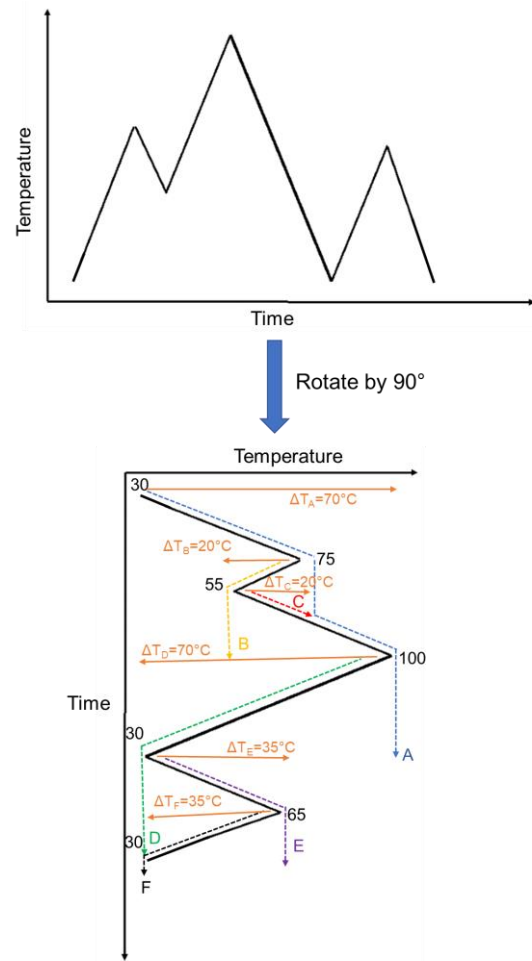


Figure 12. Theory of rainflow cycle counting.

4.2 Miner's damage accumulation rule

Miner's rule is a cumulative fatigue damage method used to estimate the lifetime of a component subjected to different load or temperature cycling conditions. In power devices, each thermal cycle causes thermomechanical stress due to expansion and contraction of materials. Repeated cycling gradually consumes the fatigue lifetime of the device.

The main idea is that every type of operating cycle consumes a fraction of the available lifetime. The total damage is obtained by adding the damage fractions from all cycle types.

The damage caused by one cycle type is:

$$D_i = \frac{n_i}{N_{f,i}}$$

where D_i is the damage fraction caused by cycle type i , n_i is the actual number of applied

cycles of type i , $N_{f,i}$ is the allowable lifetime (from PC/TC reliability diagram) in cycles of type i under the same PC/TC cycling condition.

For multiple cycle types, the total accumulated damage is:

$$D = \sum_{i=1}^m \frac{n_i}{N_{f,i}}$$

Failure, or end of predicted lifetime, is assumed when [7]:

$$D = 1$$

The lifetime of power module in terms of operational hours is calculated by dividing the time of one mission profile to the total damage caused by one mission profile.

$$Lifetime_{(PC/TC)} = \frac{t_{mission\ profile}}{D_{(PC/TC)}}$$

The least reliable interconnection and soldering component determines the overall lifetime of the power module.

Miner's rule is an engineering approximation. It assumes that fatigue damage accumulates linearly. In reality, the order of cycles, interaction between different stresses, material ageing, humidity, vibration, and manufacturing variation can also affect lifetime. Therefore, Miner's rule is useful for lifetime estimation, but it should not be treated as an exact prediction of failure time.

4.2.1 Example 1

The T_c load profile analysed previously in rain-flow counting algorithm section given in **Figure 12**, is used to calculate the damage and lifetime consumption.

As seen in the TC diagram of DIM1500ASM45-RT501 IGBT module, shown in **Figure 13**:

- 40100 cycles are for $\Delta T_c = 70^\circ\text{C}$,
- 100200 cycles are for $\Delta T_c = 35^\circ\text{C}$,
- 225000 cycles are for $\Delta T_c = 20^\circ\text{C}$.

Thus, the total damaged caused by these cycles of one mission is:

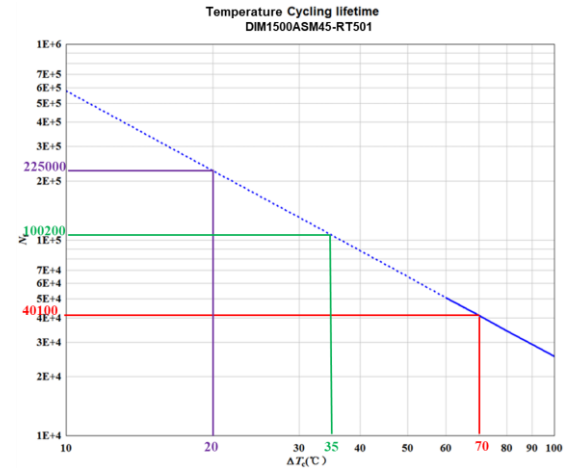


Figure 13. Example of reliability quantification from TC diagram.

$$D = \frac{1}{40100} + \frac{1}{100200} + \frac{1}{225000} = 0.0000393$$

The total number of mission profiles to cause failure i.e., $D=1$ are 25405. Thus, the module can survive 25405 mission profiles before failure.

4.2.2 Example 2

The DIM1500ASM45-RT501 IGBT power module is used in a traction application with varying load pulses per cycle as shown in **Figure 14**.

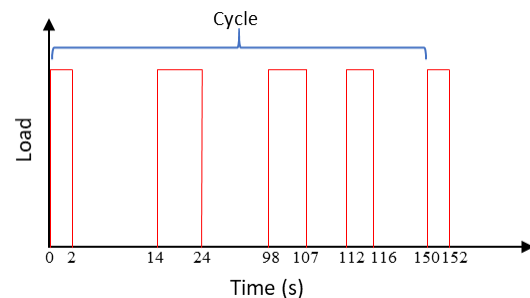


Figure 14. Exemplar operation of a power module in traction application.

The T_j rise during these pulses are as follows:

- time: 0-2s; $T_j = 25^\circ\text{C} - 57^\circ\text{C}$; $\Delta T_j = 32^\circ\text{C}$
- time: 14-24s; $T_j = 52^\circ\text{C} - 92^\circ\text{C}$; $\Delta T_j = 40^\circ\text{C}$
- time: 98-107s; $T_j = 56^\circ\text{C} - 92^\circ\text{C}$; $\Delta T_j = 36^\circ\text{C}$
- time: 112-116s; $T_j = 60^\circ\text{C} - 102^\circ\text{C}$; $\Delta T_j = 42^\circ\text{C}$

The PC diagram in **Figure 15** shows:

- 7.1×10^7 cycles for $\Delta T_j = 32^\circ\text{C}$,
- 3.1×10^7 cycles for $\Delta T_j = 36^\circ\text{C}$,

- 1.7×10^7 cycles for $\Delta T_j = 40^\circ\text{C}$,
- 1.1×10^7 cycles for $\Delta T_j = 42^\circ\text{C}$.

However, the PC diagram is for $t_{on}=3\text{s}$, and for 2s, 9s, 10s and 4s t_{on} during application of module derating factors of 1.27, 0.62, 0.6 and 0.88 respectively from **Figure 15** should be applied. This results in 90170000, 19220000, 10200000 and 9680000 cycles respectively. The total damage caused by these cycles is:

$$D = \frac{1}{90170000} + \frac{1}{19220000} + \frac{1}{10200000} + \frac{1}{9680000} \\ = 0.00000026$$

The total PC lifetime of the power module will be:

$$\text{Lifetime}_{\text{module}} = \frac{1}{D} \\ = \frac{1}{0.00000026} \\ = 3846154 \text{ Missions}$$

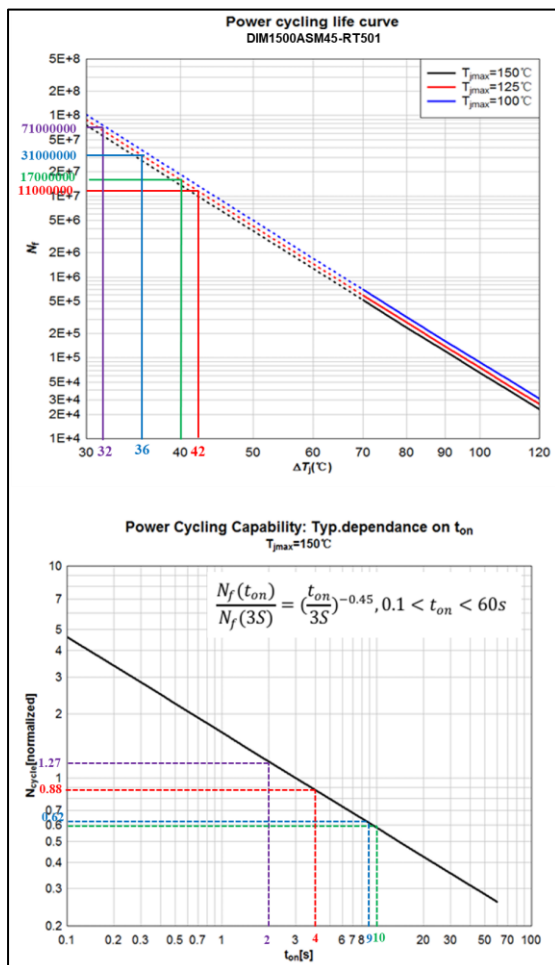


Figure 15. Example of estimating power module lifetime from PC diagram.

4.2.3 Example 3

As a fictive example, DIM1500ASM45-RT501 IGBT module is used in a train application with following assumptions:

- Train operation: 350 days per year, 18 hours per day.
- Daily service: 6 end station to end station journeys, each lasting 3 hours including 3 intermediate stations.
- Apart from partial-load cycles during cruising and coasting, the train performs 24 acceleration phases with maximum load per day (4 per end station to end station journey).
- Acceleration phase with maximum load lasts 40s.
- During the acceleration phase, the module's junction temperature is $T_j=83.6^\circ\text{C}$, case temperature is $T_c=64.1^\circ\text{C}$, and heat sink temperature is $T_h=43.6^\circ\text{C}$. Thus, $\Delta T_j=40^\circ\text{C}$ and $\Delta T_c=20.5^\circ\text{C}$ during acceleration phase.
- Daily average environment temperatures (outside train) is 25°C . During train operation, the daily average junction temperature T_j is 75°C , and the daily average case temperature T_c is 55°C , thus:
 $T_j=25^\circ\text{C}$ to 75°C ; $\Delta T_j=50^\circ\text{C}$ (daily average)
 $T_c=25^\circ\text{C}$ to 55°C ; $\Delta T_c=30^\circ\text{C}$ (daily average)

The station to station cycle can be roughly described by rise to maximum temperature during the acceleration phase with maximum load.

The PC diagram of module in **Figure 16** shows 1.98×10^7 cycles for $\Delta T_j=40^\circ\text{C}$ during acceleration phase. However, the result corresponds to $t_{on}=3\text{s}$. For acceleration phase with $t_{on}=40\text{s}$, a derating factor of 0.31, obtained from **Figure 16**, should be applied. This results in lifetime of 6.13×10^6 cycles.

For daily average T_j cycle, **Figure 16** indicates a lifetime of 5×10^6 cycles at $\Delta T_j=50^\circ\text{C}$. However, the result corresponds to $t_{on}=3\text{s}$. Considering the viscoplastic deformations saturate, the derating factor for $t_{on}=18$ hours will be 0.0112, which is calculated using the equation from the t_{on} -dependency plot in **Figure 16**. This results in lifetime of 56036 cycles.

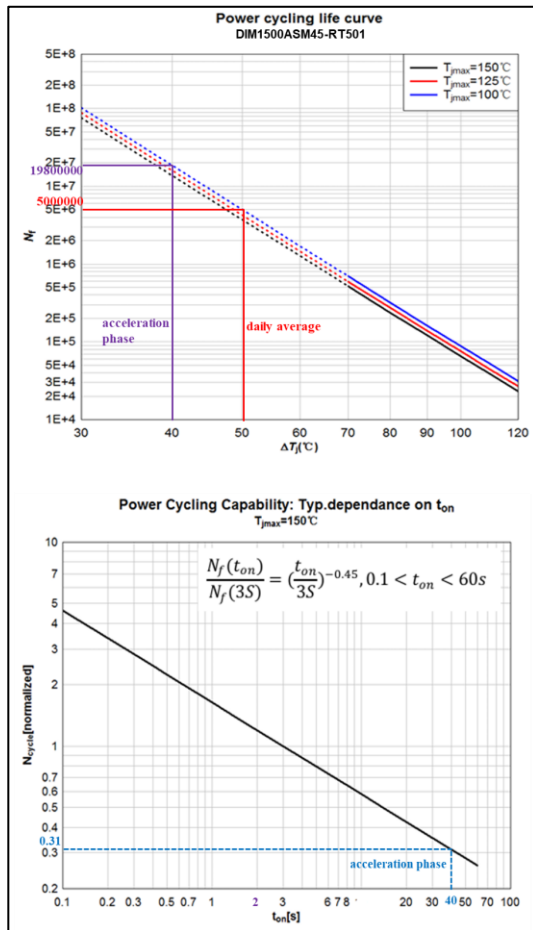


Figure 16. Example of estimating power module lifetime from PC diagram.

Thus, the total damage per day caused by 24 acceleration phases and one daily average T_j cycle will be:

$$D = \frac{24}{6.13 \times 10^6} + \frac{1}{56036} = 0.0000217$$

The total PC lifetime of the power module will be:

$$\begin{aligned} \text{Lifetime}_{PC} &= \frac{1}{D} = \frac{1}{0.0000217} \\ &= 45940 \text{ days} \end{aligned}$$

Thus, the estimated PC lifetime for 350 days per year operation of train will be 131 years.

As shown in the TC diagram of module in **Figure 17**, the lifetime is 220000 cycles for $\Delta T_c = 20.5^\circ\text{C}$ during acceleration phase, and 140000 cycles for $\Delta T_c = 30^\circ\text{C}$ for daily average T_c cycle. Therefore, the total damage per day

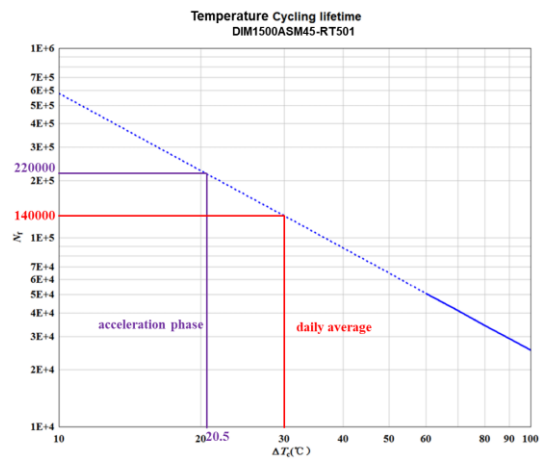


Figure 17. Example of estimating power module lifetime from TC diagram.

caused by 24 acceleration phases and one daily average T_c cycle will be:

$$D = \frac{24}{220000} + \frac{1}{140000} = 0.000116$$

The total TC lifetime of the power module will be:

$$\text{Lifetime}_{TC} = \frac{1}{D} = \frac{1}{0.000116} = 8603 \text{ days}$$

Thus, the TC lifetime prediction for 350 days per year operation of train will be 25 years.

5 Power module lifetime estimation at Dynex

If further assistance with power module lifetime estimation is required after reviewing sections 1-4, Dynex can provide additional support. Based on the intended application, operating conditions and required service lifetime, thermal and lifetime simulations can be performed at Dynex to estimate the expected module lifetime and recommend the most suitable power module to customers.

6 References

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