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AN6148
Thyristor Gate Drives
Application Note

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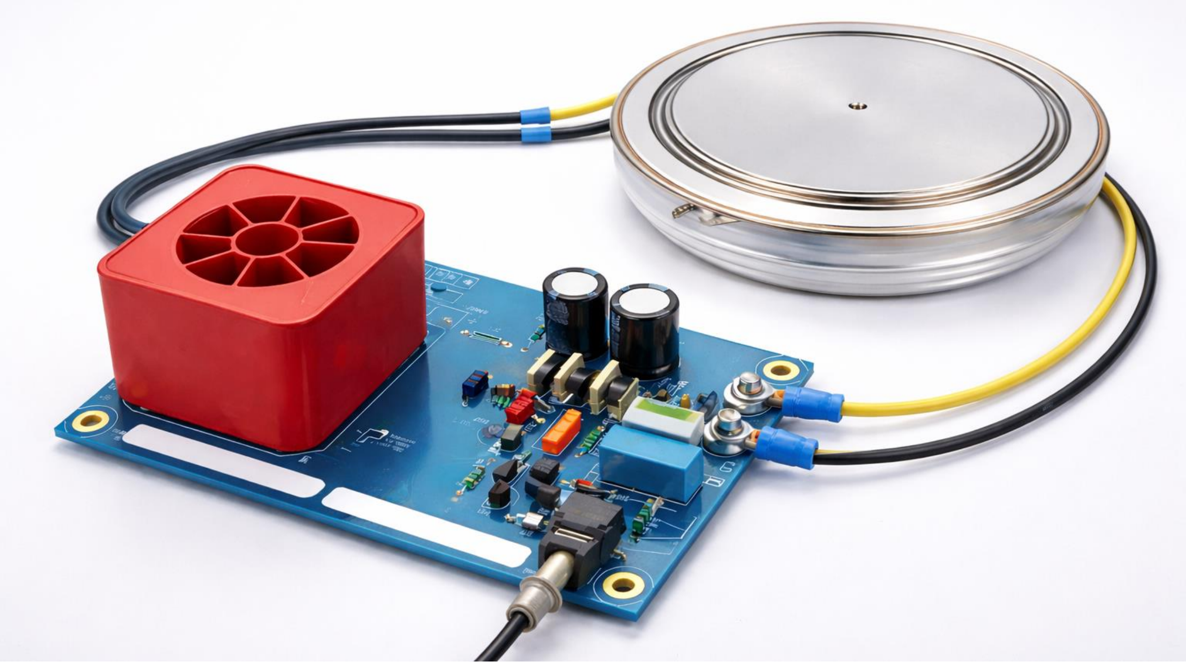

Abstract—This application note provides a practical guide to designing robust and reliable gate-drive circuits for Dynex thyristors. It outlines the fundamental operating principles of thyristor triggering, including gate current requirements, di$_T$/dt considerations, dv/dt immunity, and co-ordination with the device's thermal and electrical limits. Key aspects of driver design—such as gate-pulse shaping, isolation requirements, protection features, and interface considerations—are discussed to help engineers achieve consistent and repeatable turn-on performance across a wide range of applications. To support practical adoption, an exemplar gate-driver schematic with its required design guidelines is included at the end of the note.

1 Introduction

The output of the electronics that control the firing sequence of thyristors is typically logic-level: only a few volts, negligible current, and usually referenced to ground. In contrast, the thyristors themselves require a firing signal of tens of volts and tens to hundreds of milliamps, often applied to devices operating at high potential above ground. Bridging these widely differing electrical conditions is the role of the gate-drive circuit.

The gate-drive's purpose is to deliver a gate-current pulse with the correct shape, peak amplitude, duration, and repetition rate when commanded by the control electronics and these should be in coordination with the device's thermal and electrical limits. Additionally, each gate-drive output must be galvanically isolated, as the thyristors within a converter can differ in potential by many hundreds of volts. Triggering should also be inhibited whenever the anode voltage is negative.

Although these requirements may appear straightforward, meeting all of them reliably under real operating conditions is far from trivial. This is especially true when considering the different gate structures used in various thyristor designs. In the following sections of this application note, we examine each requirement in detail and discuss practical methods for achieving them effectively. To support real-world implementation, an example gate-driver schematic is also included at the end of the document.

2 Turn-on process of a thyristor

The turn-on process of a thyristor begins when a gate pulse is applied and the gate current starts to rise as shown in **Figure 1**. The rise time, t_r, is the period over which the gate current, i_G, increases from 10% to 90% of its peak value, I_{GM}, and during this interval the gate-current slope, di_G/dt, is important for rapidly injecting carriers into the gate region.

As the gate current builds up, the device remains in the blocking state until the internal charge distribution becomes sufficient to initiate conduction. The gate-delay time, t_{gd}, is defined as the interval between the start of the gate pulse (from 10% of I_{GM}) and the point at which the anode voltage, V_D, has fallen to 90% of its initial value.

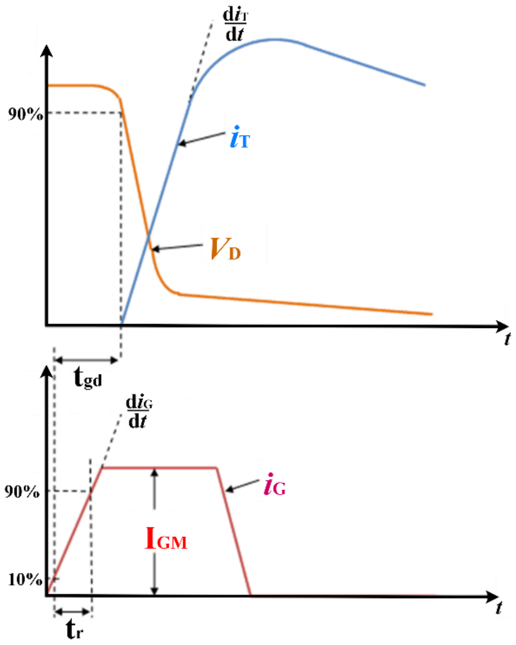

Figure 1. Thyristor turn-on process.

After t_{gd}, the thyristor transitions into full conduction: the anode current, i_T, rises with a characteristic di_T/dt, which must be supported by a strong gate drive to avoid localised current crowding, while at the same time the device voltage, V_D, collapses rapidly as the conduction area expands across the junction. The initial peak gate current, I_{GM}, helps to ensure a uniform and safe turn-on, especially in larger devices.

Altogether, these parameters (t_r, di_G/dt, t_{gd}, di_T/dt and I_{GM}) describe the dynamic behaviour of the gate signal and the thyristor current during turn-on and determine how quickly and safely the device transitions from blocking to full conduction.

3 Gate structure in high-power thyristors

The gate structure of a thyristor plays a critical role in determining its sensitivity, turn-on robustness, required gate-drive current, and overall controllability. Although many variations exist depending on wafer diameter, voltage class, and manufacturer-specific design, industrial high-power thyristors predominantly use two main gate structures: the Direct Gate Structure and the Amplifying Gate Structure.

3.1 Direct gate structure

As shown in **Figure 2**, a direct gate thyristor uses a single PN junction between the gate and cathode, with the gate region directly connected to the internal p-layer. When the gate receives a positive current pulse, it injects carriers straight into the main junction, initiating turn-on. In thyristors with a direct gate structure, turn-on performance is more strongly influenced by the gate-current pulse, as the external trigger unit must supply the entire trigger energy required to drive the thyristor into conduction.

Key characteristics of direct gate structure include:

- Simple structure with one primary gate-cathode junction.
- Requires a high level of gate current (energy) with a high di_G/dt.
- More complicated (higher power) gate driver is required.
- Turn-on begins locally where gate current is injected.
- Lower di_T/dt capability at low gate trigger energy.
- Common in lower-current (smaller) and general-purpose phase control thyristors.

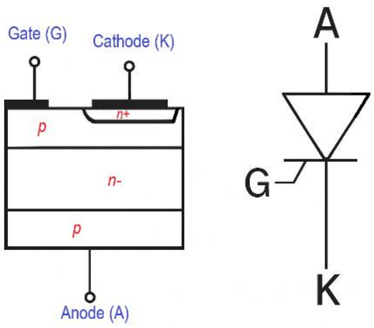

Figure 2. Thyristor general physical structure with a direct gate technology.

3.2 Amplifying gate structure

Triggering high current large thyristors demands a very high-power gate pulse, and it takes a relatively long time for the entire device to transition into full conduction. To reduce the required gate-drive effort, modern high-power thyristors incorporate amplifying-gate thyristors within the inner gate region, which is shown in **Figure 3**. In an amplifying-gate thyristor, the gate is not driving the main junction directly. Instead, the device includes an additional internal transistor-like region that amplifies the gate current before it reaches the main thyristor structure. This ensures a much stronger and more distributed triggering action.

As shown in **Figure 3**, only the amplifying-gate thyristor needs to be externally triggered, and it requires only a relatively small gate current. After this initial triggering, the amplifying-gate thyristor utilises the anode-to-cathode voltage (circuit energy) to drive the main gate region. Because of this internal amplification, thyristors with an amplifying gate are far less sensitive to weak gate current, as most of the required trigger energy is generated internally from the anode voltage.

The amplifying-gate thyristor structure can also be distributed across the entire cathode-side area using gate fingers, thereby accelerating the spread of the conducting region during turn-on, which in turn increases the device's di_T/dt capability even further.

The main concern with the amplifying-gate structure is that the auxiliary amplifying-gate thyristor is exposed to the full di_T/dt of the main circuit as soon as it begins to conduct. This di_T/dt stress gradually reduces as the main thyristor takes over and the device transitions into full conduction. This behaviour can lead to certain triggering issues, which will be discussed in Section 4.4.

Key characteristics of an amplifying-gate structure include:

- Low gate current (energy) is needed.
- Simpler gate driver is required.
- Very uniform turn-on.
- Much faster turn-on spreading.
- Higher di_T/dt capability at low gate trigger energy.
- Suitable for high-power (bigger) disc thyristors.

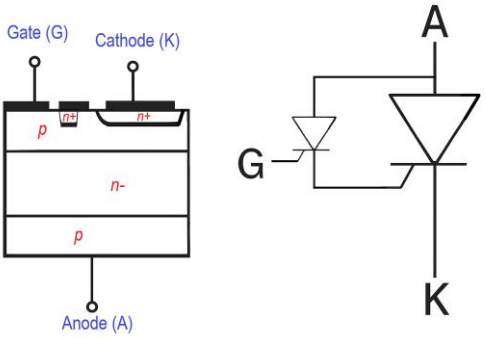

Figure 3. Thyristor general physical structure with an amplifying-gate technology.

4 Triggering thyristors

4.1 Triggering current shape

Almost any shape of current pulse will turn a thyristor into conduction as long as it exceeds the gate trigger voltage, V_{GT}, and gate trigger current, I_{GT}, values given in the datasheet. However, thyristors may need a gate current pulse with specific characteristics based on the applications and switching conditions.

Thyristors may experience high rates of rise of anode/cathode current (di_T/dt) from the discharge of the RC snubber circuit every time the thyristor is fired and from the commutation of other thyristors in the converter. Additionally, if thyristors are connected in series or parallel, they need to be turned on simultaneously. Therefore, a gate driver should be designed to provide high di_T/dt capability, low delay time, and low switching losses at the turn-on for the thyristors.

This reduction in delay time and the switching losses and the ability to receive a high di_T/dt is enhanced by the gate current pulse having a sharply rising front edge with a high rate of rise (di_G/dt), and a high peak value.

The duration of the gate pulse has to be long enough for the anode current in the thyristor to reach the Latching Current, I_L, specified in the datasheet or the thyristor might drop out of conduction when the gate signal is removed. Typically, 100µs to 150µs is adequate to allow for delay, turn-on and spreading times.

To reduce the load on the gate driver, the peak gate current does not need to be maintained for more than 10–20 µs. After this period, it can be reduced to a lower level of 2 to 4 times the I_{GT} value, known as the back-porch current.

In **Figure 4** and **Table 1**, a suitable gate pulse current for Dynex thyristors is presented. As shown, the gate current initially rises to the peak gate current, I_{GM}, and after a few microseconds it reduces to the back-porch current, I_{GB}, which is maintained for a longer period depending on the application and the conduction duration of the thyristor.

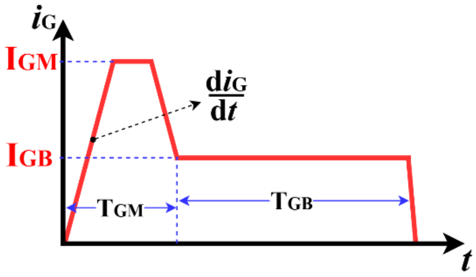

Figure 4. A typical gate pulse for Dynex thyristors.

Although with many power circuits a pulse of 100µs to 150µs is sufficient to turn the thyristor on and maintain it in conduction, some circuits require the gate current to continue throughout the conducting period, while in other cases a train of short pulses during the conduction period is sufficient (see Section 4.2).

Applying a gate trigger when the thyristor is in the reverse-blocking state will not turn it on, as the device cannot be activated under reverse-biased conditions. However, usually triggering is inhibited when the anode voltage of the thyristor is negative. This is because, in that mode, the thyristor acts like a low gain transistor and amplifies the gate current which is seen as an increase in anode leakage current. This, together with the blocking voltage across the device, gives a significant increase in power dissipation in the thyristor. The extra power loss has to be considered when dimensioning the heat-sinks, otherwise the device can overheat. But perhaps its most significant effect is associated with series connected thyristors where the increase in leakage current can make achieving voltage sharing between the thyristors much more difficult.

Table 1. Gate pulse characteristics for Dynex thyristors.

Parameter	Recommended value	Considerations
Peak initial gate current, I_{GM}	5-10 × I_{GT}	Higher di_T/dt or/and larger thyristors require higher I_{GM}.
Duration of initial peak gate current, T_{GM}	10–20 µs	Larger thyristors require longer T_{GM}. Very low di_T/dt values (<5A/µs) also require an increased T_{GM}.
Back-porch peak current, I_{GB}	2-4 × I_{GT}	Larger thyristors require higher I_{GB}.
Duration of back-porch gate current, T_{GB}	100–150 µs	Larger thyristors require longer T_{GB}. T_{GB} can be shorter than 100 µs in applications where the thyristor conducts only for a short duration with a very high di_T/dt, such as pulse power systems.
Rate of rise time of the gate current di_G/dt	>1 A/µs	Higher di_T/dt or/and larger thyristors require higher di_G/dt. In pulse-power applications, the required di_G/dt is much higher and may need to even exceed 20 A/µs. In the Dynex datasheet, where the di/dt rating is defined, the required di_G/dt (= I_{GM}/t_r) for the provided di/dt range is also mentioned in the test conditions.
Gate driver open circuit voltage, V_{GO}	>12 V	The higher the di_T/dt, the higher the required V_{GO}. For amplifying-gate thyristors (most of Dynex thyristors) and the thyristors used in pulse power applications, a source voltage greater than 24 V may be required. For case temperatures, T_C, below 0°C, V_{GO} should be greater than 30 V.

4.2 Triggering power losses

The anode-cathode voltage may temporarily reverse during the conduction period or there may not be positive volts present at the initial point of firing. In the extreme, in the case of an AC converter with an inductive load for instance, a pulse duration of 180°- α is required, where α is the thyristor firing (phase-delay) angle measured from the AC voltage zero crossing, i.e. up to 10ms for 50Hz. The most suitable system depends upon the power circuit being employed. However, the gate pulse should only be made as long as is necessary, because the magnitude of the average gate power has to be considered. The longer the gate pulse, the higher the average power which may lead to additional heating and possible destruction of the thyristor.

Dynex Application Notes AN4840 and AN6196 [1], [2] discuss the use of gate-drive load lines together with the thyristor gate current–gate voltage characteristics to ensure that the gate-driver power does not exceed the device limitations. These gate-voltage characteristics must be strictly followed in the gate-pulse design, especially if the application is expected to operate close to the device limits. In addition, in practice it is uneconomic to produce gate drives with very long pulses for reasons of gate driver power requirements and availability of pulse transformers.

To reduce the power losses on the gate and also the power requirement of the gate driver, a chain of short pulses with a frequency in the region of 5kHz to 10kHz may be used as presented in **Figure 5**. This is sometimes called a "picket fence" waveform. If the gaps between the pulses cause interference, a second time shifted pulse chain can be superimposed to produce a continuous long pulse. The pulse transformer only has to be dimensioned for a single pulse in the chain, say 50µs to 100µs.

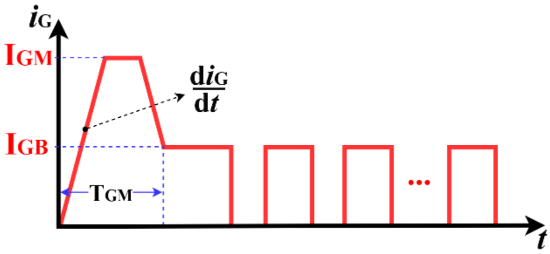

Figure 5. Short gate pulse picket fence.

4.3 High di_T/dt considerations

At the moment a thyristor begins to conduct, only a small portion of the device area around the gate is active. In most line-commutated circuits this does not pose a problem because the thyristor current increases at a low di_T/dt rate, giving the conduction area time to spread accordingly.

In contrast, there are many applications such as pulse power converters that can impose repetitive fast current rise rates or single pulses with both steep di_T/dt and high peak current. In such cases, the conduction area may not expand quickly enough, causing the initial current to be concentrated near the gate region. This part of the device typically has less effective cooling due to the gate structure, making it more vulnerable to local overheating and potential failure.

Delivering a strong initial gate pulse promotes uniform triggering of both the amplifying-gate region and the main junction. This leads to rapid spreading of conduction area and helps the device safely withstand its highest rated di_T/dt. In this context, a strong gate pulse refers to an initial peak current, I_{GM}, exceeding 10 × I_{GT} with a rise time, t_r, of less than 1.5 µs.

Even in applications where the circuit di_T/dt is expected to be low, the actual turn-on di_T/dt experienced by the thyristor can be significantly higher due to the presence of snubber capacitors, voltage-balancing/protection/dividing capacitors, and parasitic capacitances within the circuit and the cables. These capacitors can discharge rapidly at the instant of the thyristor turn-on, adding an additional current component on top of the main circuit current. As a result, the thyristor may experience a much higher effective di_T/dt during the initial turn-on interval than the di_T/dt of the main circuit would suggest. Therefore, if a higher di_T/dt is anticipated due to the presence of these capacitors, the initial gate pulse should be made sufficiently strong to ensure that the conduction area spreads quickly and uniformly within the device.

4.4 Gate driver voltage for thyristors with amplifying gates

The dynamic voltage drop across the gate-to-cathode, $V_{GT}(t)$, depends on the charge-carrier concentration, internal inductances, and the di_T/dt of the anode current.

At the start of conduction—when the gate region is not yet fully flooded with carriers—the effective gate-to-cathode impedance is higher than its steady-state value. In addition, in thyristors with an amplifying-gate structure, the distributed resistance within the amplifying-gate region, R_{AG}, produces an additional internal voltage drop during turn-on. The combined effect of the higher initial impedance and the R_{AG}-related drop results in a larger instantaneous $V_{GT}(t)$ for the same gate-current level compared to its steady-state value. This effect becomes particularly significant when the thyristor experiences a high di_T/dt.

At the beginning of the thyristor turn-on process, when the circuit di_T/dt is high, the amplifying-gate section conducts a large current to trigger the main junction. This current flows through the auxiliary amplifying path and further increases the dynamic gate-to-cathode voltage due to the additional voltage drop across the amplifying gate path's internal impedance. Because this internal voltage couples back to the gate-driver terminals, the external gate current can momentarily dip if the gate driver's open-circuit voltage, V_{GO}, is not sufficiently high (see **Figure 6**).

A high main-circuit di_T/dt can stress or even damage the auxiliary thyristor during the early turn-on phase, and a gate-current dip approaching zero can significantly exacerbate this risk.

To prevent the gate-current dip from falling to a level that could weaken the turn-on of an amplifying-gate thyristor, the gate driver may need to provide a higher open-circuit gate voltage (typically with $V_{GO} > 30$ V).

As the gate behaves like a diode, there is no strict upper limit on the forward gate-cathode voltage; the practical limitation is the allowable power dissipation in the gate circuit. However, the reverse gate-cathode voltage must be kept very low (ideally close to zero) to avoid damaging the gate junction.

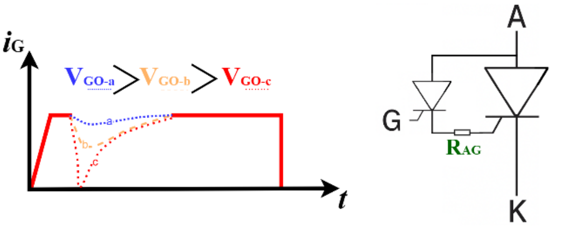

Figure 6. Gate current distortion due to steep di_T/dt in the amplifying-gate.

4.5 Series and parallel connections

For series and parallel connections, it is essential that all thyristors turn on simultaneously to ensure proper dynamic voltage and current balancing. To minimise differences in gate-controlled delay times, t_{gd}, every device in the chain should receive simultaneous, high-amplitude, and fast-rising trigger pulses—for example, 4–10 times the rated gate-trigger current, I_{GT}, with a rise time, t_r, below 1 µs (ideally below 0.5 µs). This approach reduces variation in delay time and prevents any single device from experiencing an excessive share of the total voltage or current.

For more information on voltage and current balancing in series- and parallel-connected thyristors, please refer to Dynex application note AN6531 [3].

4.6 Interference

The gate drive largely determines the performance and reliability of the equipment, and incorrect triggering can lead to severe consequences. One frequent cause of misfiring is electrical interference coupled into the firing circuit from the power stage or from relays and contactors located nearby.

To improve noise immunity, it is advisable to include components such as blocking diodes, capacitors and earth screens on the pulse transformers. Because thyristors typically operate in electrically noisy environments, the inductance of the gate leads should be kept as low as possible by mounting the gate driver close to the device and by twisting the gate leads or using coaxial cables. Care must also be taken to ensure that gate leads do not run close to high-voltage or high-current conductors, as this can lead to electromagnetic interference or, in extreme cases, flash-over.

In applications with particularly high levels of electrical noise or long distances between the control electronics and the gate driver, using a fibre-optic firing command can significantly improve noise immunity and eliminate many coupling-related issues.

5 Gate driver topologies

As mentioned at the beginning of this application note, thyristors operate at line potential, whereas the control system is typically a low-voltage circuit referenced to ground. Therefore, the gate signal must be galvanically isolated from the control electronics.

While gate drivers may be categorised into several voltage classes, Dynex thyristors generally operate in applications above 0.5 kV. For practical purposes, we therefore define two groups for gate-driver design:

- High-voltage systems: above 10 kV
- Medium-voltage systems: approximately 0.5 kV to 10 kV

These ranges reflect the typical operating levels of Dynex bipolar devices and their associated insulation requirements.

5.1 High voltage applications

For voltages above 10 kV, the triggering design becomes more complex due to the critical nature of applications such as HVDC systems. If electrical triggering is used, the triggering energy should be derived from the main circuit rather than from a separate energy source for each gate driver. This is because the required insulation voltage and the required high number of the gate drivers would make providing an independent energy supply for each gate driver impractical.

In these cases, the gate-drive power is typically derived from the anode–cathode potential, and the firing command is transmitted to the gate driver via an optical control signal to ensure high galvanic isolation and strong immunity to electrical noise, as shown in **Figure 7**. The anode voltage is electrically transferred to a switched-capacitor circuit within the gate driver. The switched-capacitor circuit adjusts the required voltage level and current shape for triggering and delivers the necessary energy to the gate when the optical command arrives.

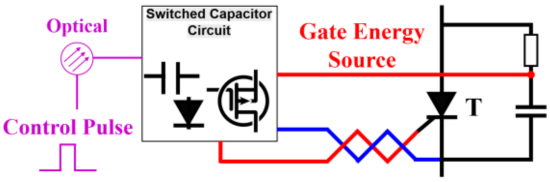

Figure 7. Thyristor gate drive using the anode voltage as the triggering-energy source.

5.2 Medium voltage applications

For applications below 10 kV, the main-circuit energy for triggering the thyristors (**Figure 7**) can also be used, and even an electrical control pulse may be sent, although optical signalling remains the preferred method. In addition to this approach, it can also be practical to use a separate voltage source for each gate driver or for a group of gate drivers.

Gate drivers suitable for high-voltage thyristors with a separate energy source can generally be categorised into two groups, depending on whether the gate-pulse current is generated before or after isolation from the input energy source:

- Pre-isolation pulse formation using pulse transformers
- Post-isolation pulse formation using switched-capacitor/rectifier circuits

5.2.1 Pulse-transformer–based gate drivers

Using a pulse-power transformer, as shown in **Figure 8**, this type of gate drive is fully magnetic. A triggering pulse—either optical or electrical—is applied to a power semiconductor switch such as a MOSFET or IGBT on the primary side of the pulse transformer. This generates a current pulse that is transferred to the secondary side and delivered to the thyristor gate.

It should be noted that the leakage inductance of the transformer can limit the di_G/dt (i.e., increases the rise time) of the gate-current pulse. Therefore, the pulse-power transformer should be designed with minimal leakage inductance. It is not straightforward to obtain a very high di_G/dt using this type of gate driver. Hence, this gate-driver topology is generally not recommended for applications where the di_T/dt of the thyristor exceeds 300 A/µs.

The input energy channel must be isolated from the user interface by appropriate insulation. If this is not inherently provided, reinforced insulation is required for the pulse transformer (see IEC/EN 60664-1, EN 61140, or EN 50178). In addition, if the firing command (control pulse) is transferred electrically (rather than via a fibre-optic link), reinforced insulation may still be required for the pulse transformer regardless of the insulation between the user interface and the input energy. Whether this is necessary depends on the insulation performance of the electrical interface. This is because, in medium- and high-voltage applications, opto-couplers can be limited by clearance and creepage.

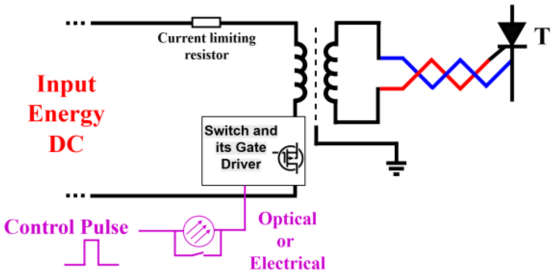

Figure 8. Thyristor gate drive based on a pulse transformer.

Finally, diodes, capacitors, and earth screening to prevent spurious triggering are also required.

5.2.2 Switched-capacitor/rectifier-based gate drivers

Using an isolation transformer for the input supply voltage, the gate driver incorporates a rectifier and a switched-capacitor circuit to store energy as shown in **Figure 9**. The switched-capacitor circuit adjusts the required voltage level and current shape for triggering. By commanding a power semiconductor switch—such as a MOSFET or IGBT—a current pulse is delivered to the thyristor gate. The firing command can again be transmitted electrically or optically; however, an optical connection is generally recommended, as it provides better synchronisation between multiple gate drivers (for series and parallel connections) and is less susceptible to interference within the circuit.

This type of gate-driver topology can deliver a very high di_G/dt (i.e., a fast rise time) for the gate-current pulse and is therefore well suited to applications that require very high di_T/dt capability, such as pulse-power systems and applications where series or parallel connections are required for the thyristors.

Again, the input energy channel must be isolated from the user interface by appropriate insulation. If this is not inherently provided, reinforced insulation is required for the input transformer (see IEC/EN 60664-1, EN 61140, or EN 50178). In addition, the firing command must be galvanically isolated from the control electronics. If it is transferred electrically, the command channel shall provide safe separation in accordance with the relevant insulation-coordination requirements. In medium- and high-voltage applications this is most reliably achieved using a magnetic pulse transducer or a fibre-optic link, as opto-couplers can be limited by clearance and creepage. Therefore, fibre-optic triggering is often the simplest route to reinforced insulation.

If adequate insulation is provided for the input-energy path and optical triggering is used, this gate driver can be applied even in systems with voltage levels well above 10 kV. However, for very high voltages (above approximately 30 kV), decoupled-energy gate drivers (**Figure 7**) is still recommended to be used.

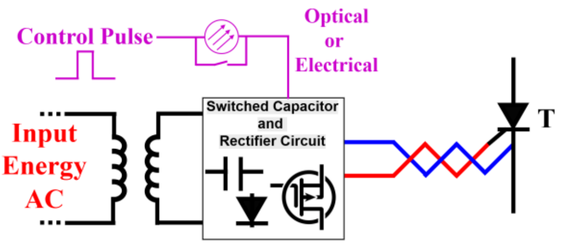

Figure 9. Thyristor gate drive based on a switched-capacitor circuit.

6 Design guidelines for a gate driver using a pulse transformer

A typical gate-driver schematic that can be used for most medium voltage applications—provided the di_T/dt does not exceed 300 A/µs—is shown in **Figure 10**.

***Input voltage**, V_{in}*: The input voltage should be selected according to the thyristor's gate technology and the required di_T/dt performance. As a general guideline, a minimum of 24 V is recommended. For applications requiring di_T/dt above 10 A/µs, the input voltage should typically be increased to a minimum of 30 V, and for very high di_T/dt requirements it may be raised to as much as 60 V.

Current limiting resistors, R_{L1}, R_{L2}, and R_{L3}: R_{L1} has the highest resistance value and is used to adjust the back-porch peak current (I_{GB}), based on the input voltage. R_{L2} and R_{L3} should have very small resistance values—typically around 1 Ω—and are used to define and shape the initial peak current.

Current limiting capacitor, C_L: This capacitor is the main contributor to the initial peak current, as it forms a resonant circuit with the leakage inductance of the transformer, thereby increasing the peak current. Its value determines the magnitude of the initial gate-current peak, I_{GM}, its duration, and the rise time of the gate-current pulse.

Noise immunity capacitor and resistor, C_f and R_f: These two components reduce the chance of misfiring caused by interference within the circuit. The filter must be designed carefully to ensure that it does not excessively attenuate the gate pulse. The RC time constant ($R_f \times C_f$) should typically be maintained between 10 and 20 µs, and a capacitance value between 10 and 47 nF is generally recommended.

Turns ratio, $N_P : N_S$: The turns ratio of the transformer defines the initial peak current and must be selected carefully; however, a 1:1 turns ratio is generally acceptable.

Voltage Time Area of the transformer: The volt–second capability of the transformer must be selected carefully to ensure it does not enter saturation. If a larger transformer is required to provide a high volt–second capacity, it will likely exhibit higher coupling capacitance. In such cases, an earthed shield between the primary and secondary windings is recommended.

Insulation voltage: The pulse transformer used in the gate driver must satisfy the insulation-coordination requirements of the application and comply with the relevant safety standards, such as IEC/EN 60664-1 and EN 61140 (or EN 50178, depending on the end-use equipment).

Reverse protection diodes, D_1 and D_2: To avoid any reverse current to the trigger circuit, the trigger circuit needs to be equipped with decoupling diodes. Note that D_2 also helps to eliminate negative gate currents that are mentioned in Section 4.4. D_1 and D_2 should be fast diodes with a low forward-voltage drop, and their blocking-voltage rating should be at least three times the input voltage and current rating above 5A. If the initial peak current exceeds 10 A, or if the pulse duration is longer than 150 µs, a diode with a higher current rating may be required.

Switching power semiconductor: It is recommended to use a MOSFET with a blocking-voltage rating of at least three times the input voltage and a current rating above 5 A. If the initial peak current exceeds 10 A, or if the pulse duration is longer than 150 µs, a MOSFET with a higher current rating may be required.

Voltage clamping circuit: This is optional but recommended in situations where the MOSFET experiences high voltage spikes during switching. A Zener diode, D_Z, with a clamping voltage of maximum up to twice the input voltage should be used, placed in series with a fast diode, D_C. The fast diode should have a blocking-voltage rating of at least three times the input voltage and a current rating above 5 A.

Gate leads: The leads between the gate driver and the thyristor gate should be kept as short as possible. It is also recommended to use coaxial cables, or at least twist the gate leads together, to improve noise immunity and reduce gate loop-inductance.

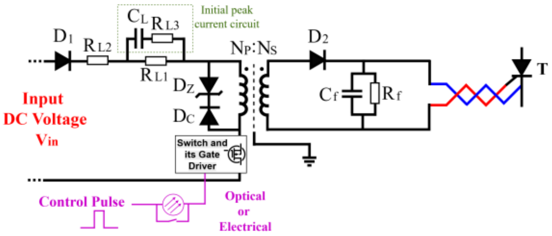

Figure 10. Thyristor gate drive based on pulse transformer with initial peak current.

7 Final remarks

In this application note, the gate drivers generally suitable for applications of Dynex disc thyristors are discussed, with a particular focus on commonly used and well-established gate-driver solutions. As a result, many other possible gate-driver implementations are not covered here. For further information on alternative approaches, please refer to [4].

Finally, for systems with voltage levels below 500 V, the gate drivers discussed above can also be used. In addition, simpler direct gate-driver solutions, with a topology similar to that shown in **Figure 9**, may be suitable. In such cases, an input transformer may not be required, and an optocoupler can be used to provide isolation for the control electronics.

8 References

[1] Dynex Semiconductor Ltd, AN4840: Gate Triggering and Gate Characteristics, Application Note, AN4840-5, Oct. 2022.

[2] Dynex Semiconductor Ltd, AN6196: Gate Power Calculations, Application Note, LN42379, Feb. 2023.

[3] Dynex Semiconductor Ltd, AN6531: Guidelines for Series and Parallel Configurations of Press-Pack Thyristors and Diodes, Application Note, LN43892, Feb. 2025.

[4] Wahl, F.P., 2002, October. Firing Series scrs at medium voltage: Understanding the topologies ensures the optimum gate drive selection. In Power Systems World Conference, Chicago, Illinois.

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