

PACKAGE OUTLINE

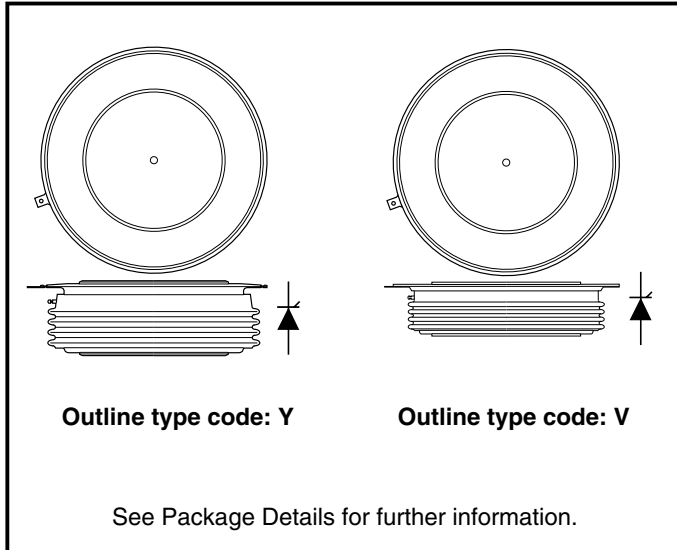


Fig. 1 Package outline

KEY PARAMETERS

V_{DRM} 5200V

$I_{T(AV)}$ 2162A

I_{TSM} 40000A

dV/dt^* 1000V/ μ s

dI/dt 300A/ μ s

*Higher dV/dt selections available

VOLTAGE RATINGS

Part Number	Repetitive Peak Voltages		Conditions
	V_{DRM}	V_{RRM}	
DCR1576SY52 or DCR1576SV52	5200	5200	$T_{vj} = 0^\circ$ to 125° C. $I_{DRM} = I_{RRM} = 500$ mA. $V_{DRM}, V_{RRM} = 10$ ms 1/2 sine. $V_{DSM} \& V_{RSM} = V_{DRM} \& V_{RRM} + 100$ V respectively.
	V		

Lower voltage grades available.

ORDERING INFORMATION

When ordering select the required part number shown in the Voltage Ratings selection table.

For example:

DCR1575SY52 for a 5200V 'Y' outline variant

or

DCR1576SV52 for a 5200V 'V' outline variant

If a lower voltage grade is required, then use $V_{DRM}/100$ for the grade required e.g.:

DCR1576SY44 for a 4400V 'Y' outline variant etc.

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS $T_{\text{case}} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2162	A
$I_{T(RMS)}$	RMS value	-	3396	A
I_T	Continuous (direct) on-state current	-	3200	A
Single Side Cooled (Anode side)				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1440	A
$I_{T(RMS)}$	RMS value	-	2261	A
I_T	Continuous (direct) on-state current	-	1984	A

CURRENT RATINGS $T_{\text{case}} = 80^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1720	A
$I_{T(RMS)}$	RMS value	-	2700	A
I_T	Continuous (direct) on-state current	-	2500	A
Single Side Cooled (Anode side)				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1120	A
$I_{T(RMS)}$	RMS value	-	1760	A
I_T	Continuous (direct) on-state current	-	1510	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine; $T_{case} = 125^{\circ}C$	32.0	kA
I^2t	I^2t for fusing	$V_R = 50\% V_{RRM} - 1/4$ sine	5.12×10^6	A ² s
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine; $T_{case} = 125^{\circ}C$	40.0	kA
I^2t	I^2t for fusing	$V_R = 0$	8.0×10^6	A ² s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.0095	$^{\circ}C/W$
		Single side cooled	Anode dc	-	0.019	$^{\circ}C/W$
			Cathode dc	-	0.019	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 50.0kN with mounting compound	Double side	-	0.002	$^{\circ}C/W$
			Single side	-	0.004	$^{\circ}C/W$
T_{vj}	Virtual junction temperature	On-state (conducting)	-	135	$^{\circ}C$	
		Reverse (blocking)	-	125	$^{\circ}C$	
T_{stg}	Storage temperature range		-55	150	$^{\circ}C$	
-	Clamping force		45.0	55.0	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Conditions	Typ.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	300	mA	
dV/dt	Maximum linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$.	-	1000	V/ μ s	
di/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$ Gate source 20V, 20 Ω $t_r < 0.5\mu$ s.	Repetitive 50Hz	-	150	A/ μ s
			Non-repetitive	-	300	A/ μ s
$V_{T(TO)}$	Threshold voltage	At $T_{vj} = 125^{\circ}C$	-	1.05	V	
r_T	On-state slope resistance	At $T_{vj} = 125^{\circ}C$	-	0.34	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, Gate source 30V, 15 Ω Rise time 0.5 μ s, $T_j = 25^{\circ}C$	-	2.5	μ s	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	550	1000	mA	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{g-k} = \infty$	150	300	mA	
t_q	Turn-off time	$I_T = 800A$, $t_p = 1ms$, $T_j = 125^{\circ}C$, $V_{RM} = 50V$, $di_{RR}/dt = 20A/\mu$ s, $V_{DR} = 67\% V_{DRM}$, $dV_{DR}/dt = 20V/\mu$ s linear	1.0	-	ms	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5V$, $T_{case} = 25^{\circ}C$	3.0	V
I_{GT}	Gate trigger current	$V_{DRM} = 5V$, $T_{case} = 25^{\circ}C$	300	mA
V_{GD}	Gate non-trigger voltage	At V_{DRM} , $T_{case} = 125^{\circ}C$	0.25	V
V_{FGM}	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V_{FGN}	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V_{RGM}	Peak reverse gate voltage		5	V
I_{FGM}	Peak forward gate current	Anode positive with respect to cathode	30	A
P_{GM}	Peak gate power	See table, fig.4	150	W
$P_{G(AV)}$	Mean gate power		10	W

CURVES

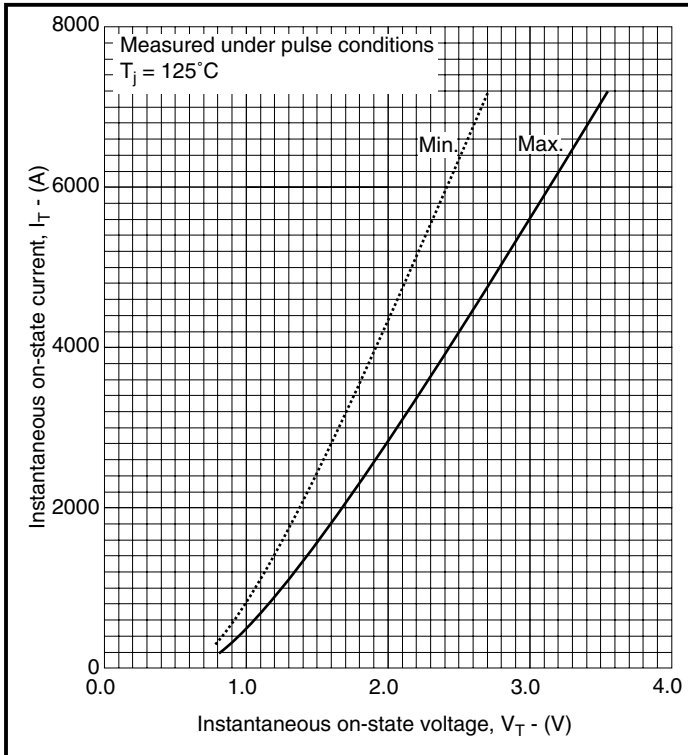


Fig.2 Maximum (limit) on-state characteristics

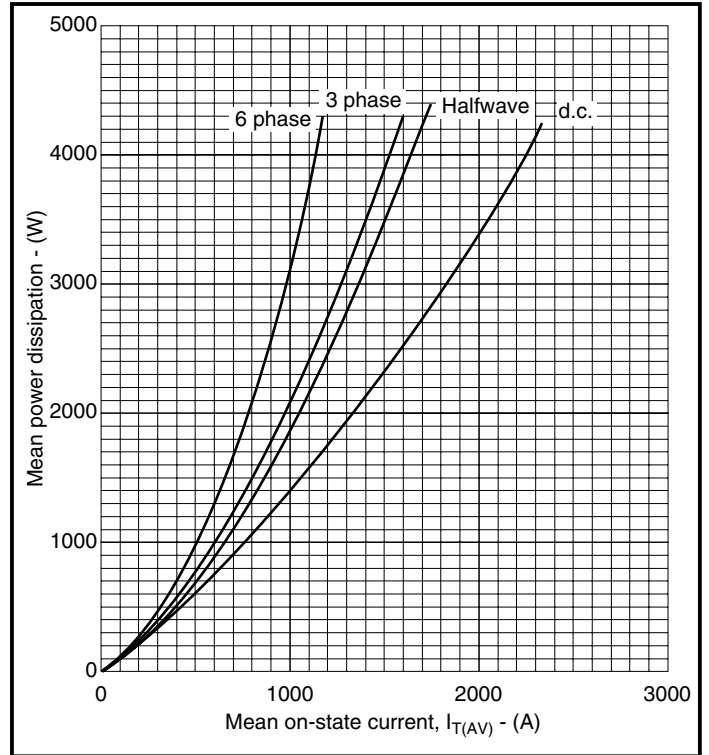


Fig.3 Dissipation curves

V_{TM} Equation:-

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where

- A = 0.414672883
- B = 0.039124962
- C = 0.000288077
- D = 0.008514638

these values are valid for $T_j = 125^\circ\text{C}$ for I_T 500A to 7200A

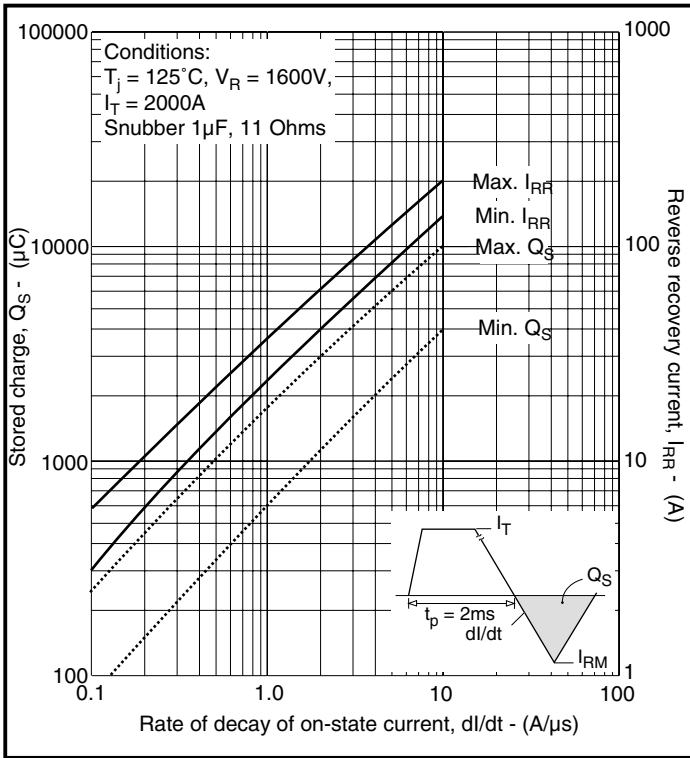


Fig.4 Stored charge

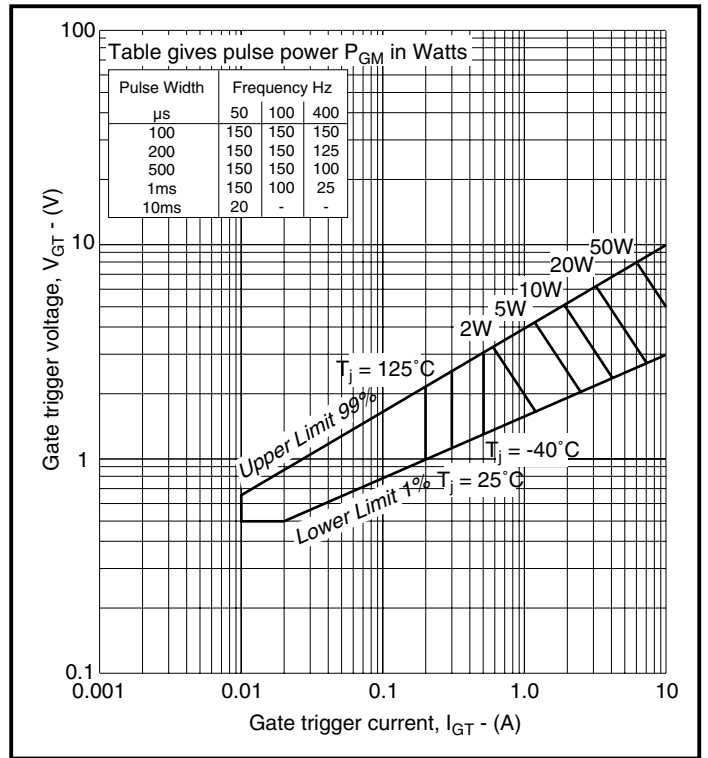


Fig.5 Gate characteristics

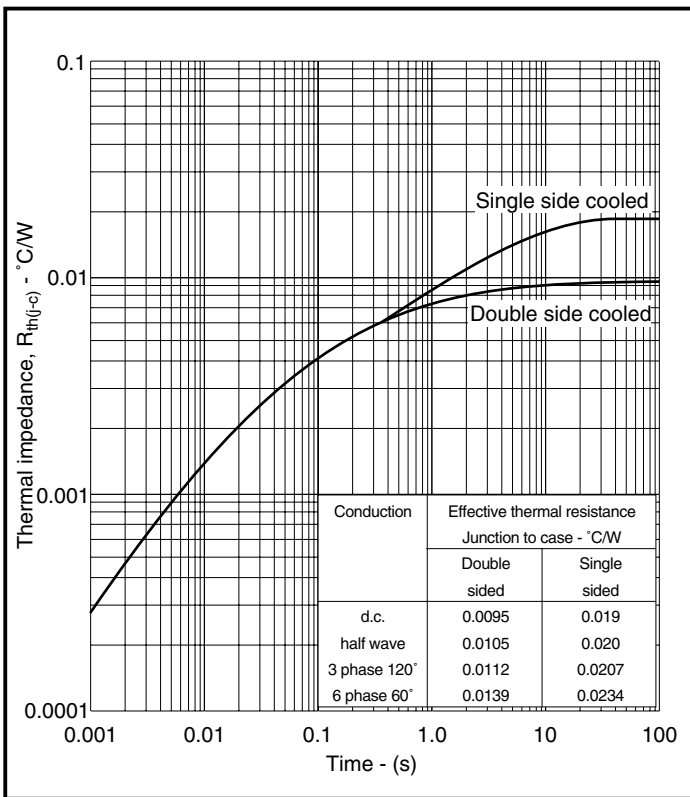


Fig.6 Transient thermal impedance - junction to case

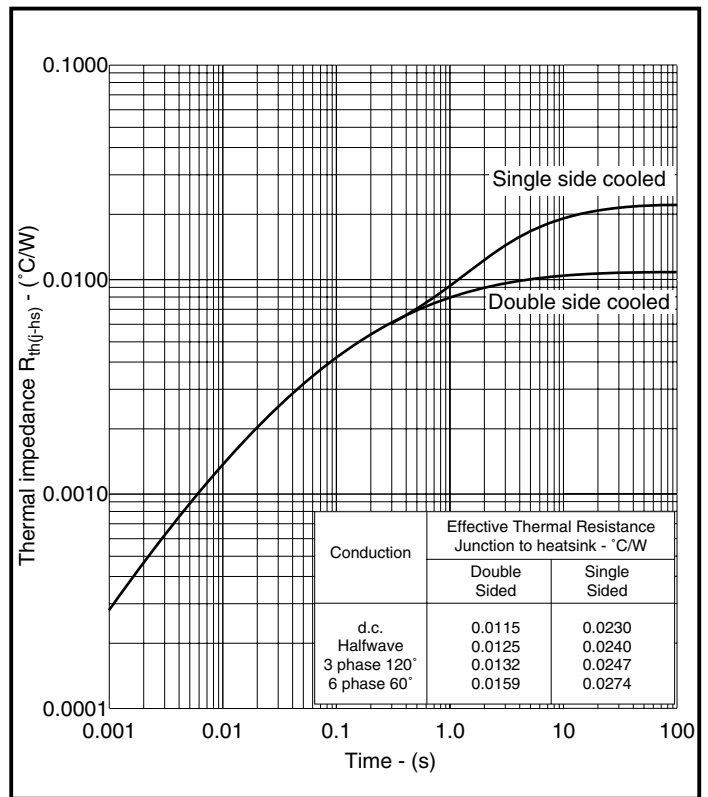


Fig.7 Transient thermal impedance - junction to heatsink

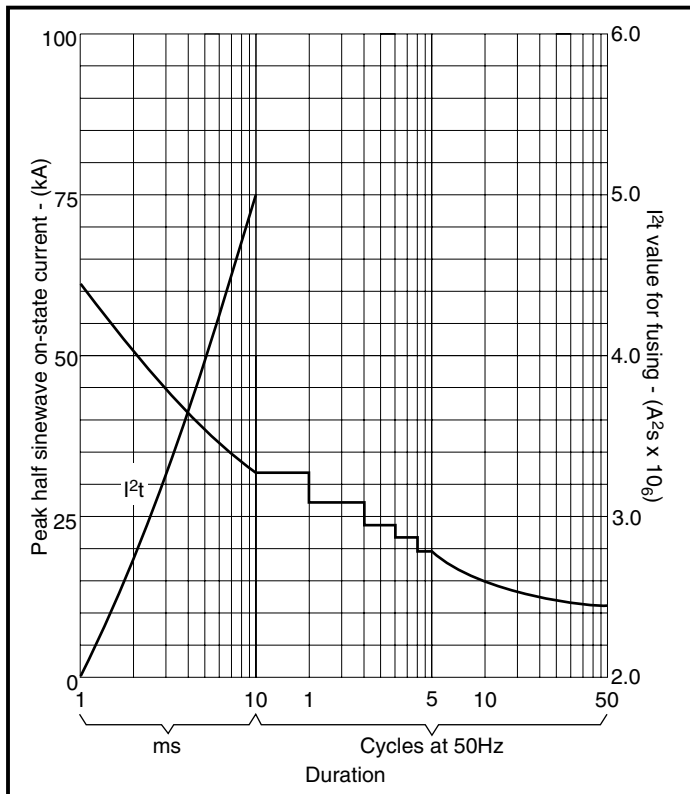


Fig.7 Surge (non-repetitive) on-state current vs time (with 50% V_{RRM} at $T_{case} = 125^\circ C$)

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

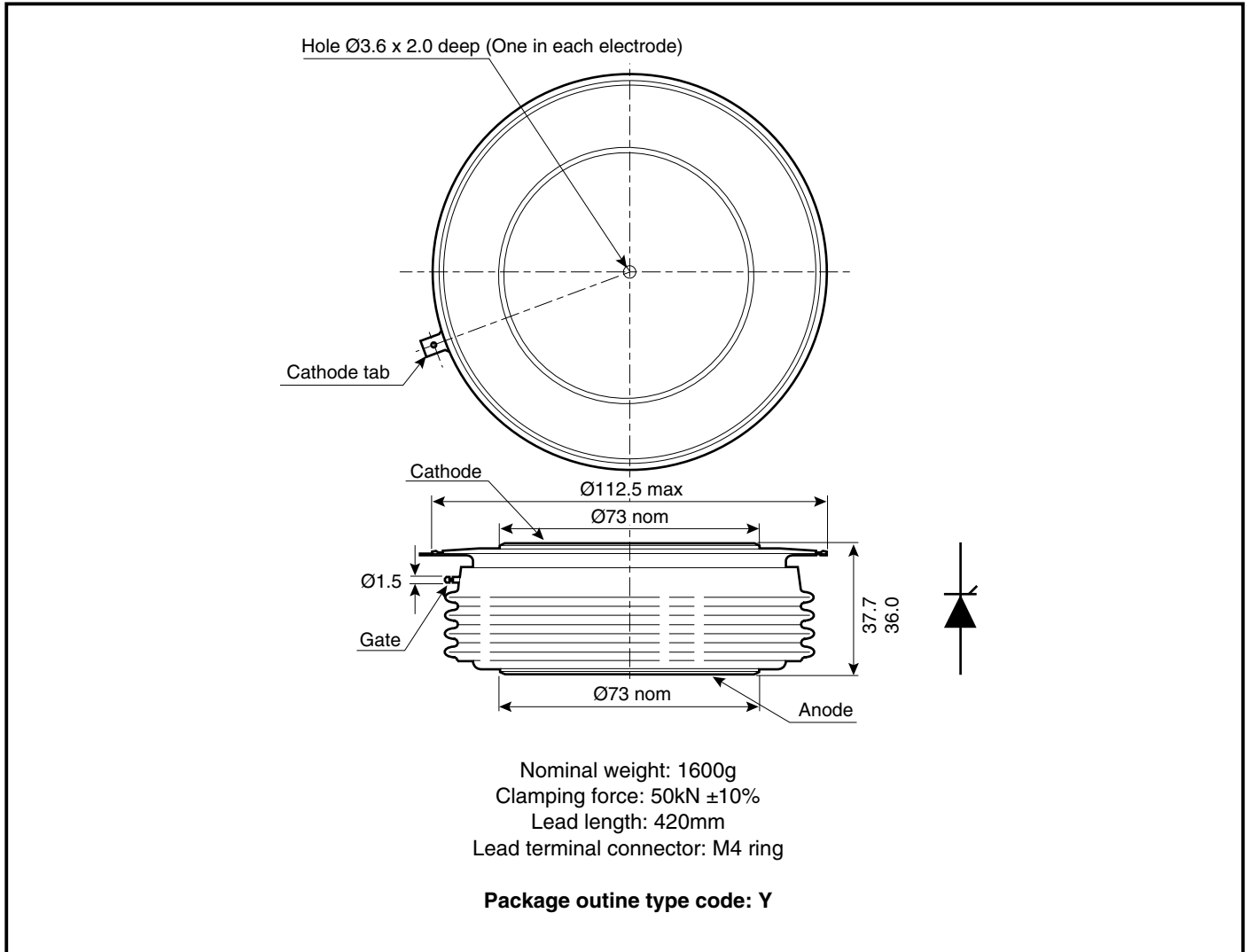


Fig.8 Package details

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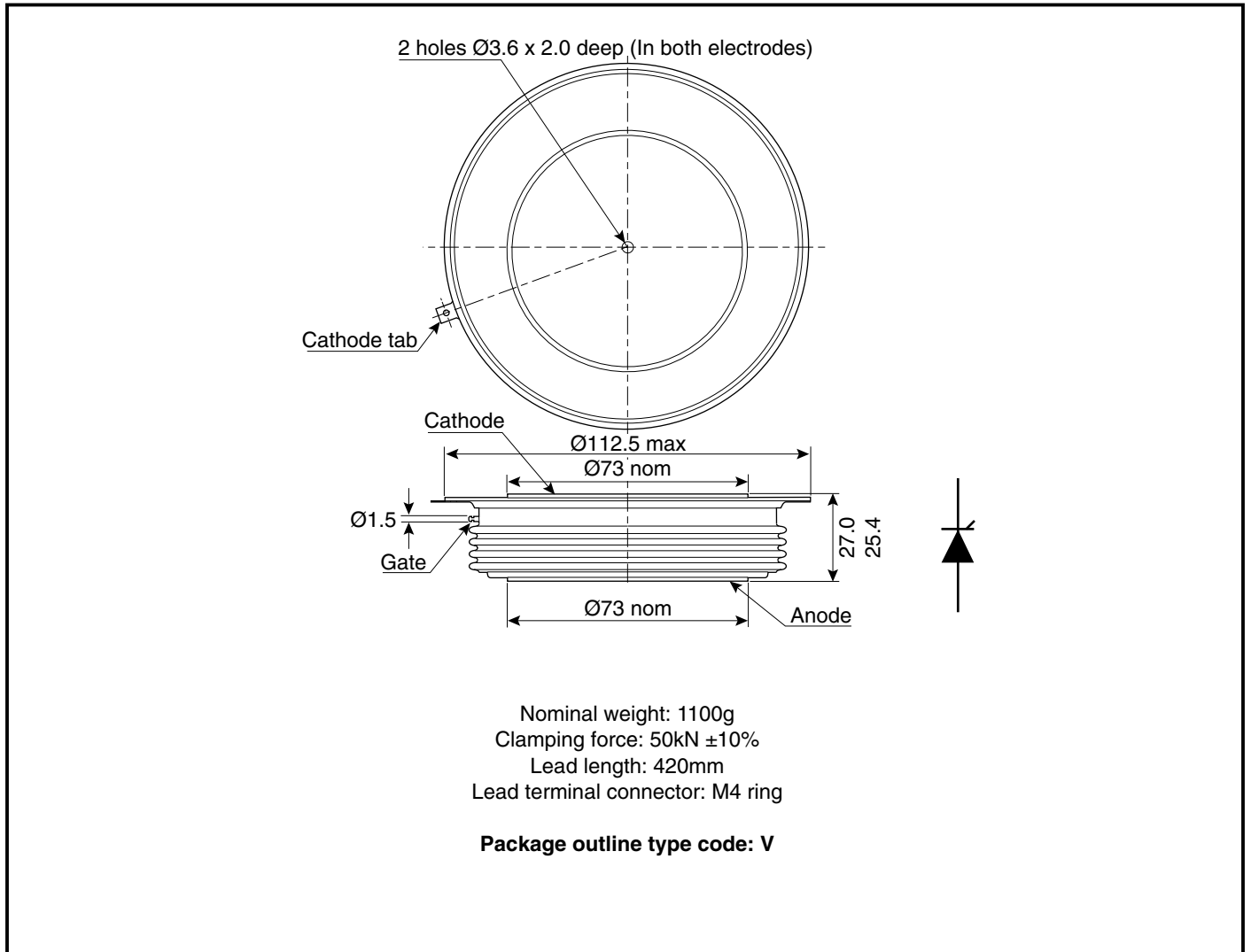


Fig.9 Package details

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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