

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR2950W65*	6500	$T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 300\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR2950W60	6000	
DCR2950W55	5500	
DCR2950W50	5000	

Lower voltage grades available.
 * 6200V @ -40°C , 6500V @ 0°C

KEY PARAMETERS

V_{DRM}	6500V
$I_{T(AV)}$	2945A
I_{TSM}	38500A
dV/dt^*	1500V/μs
dI/dt	300A/μs

* Higher dV/dt selections available

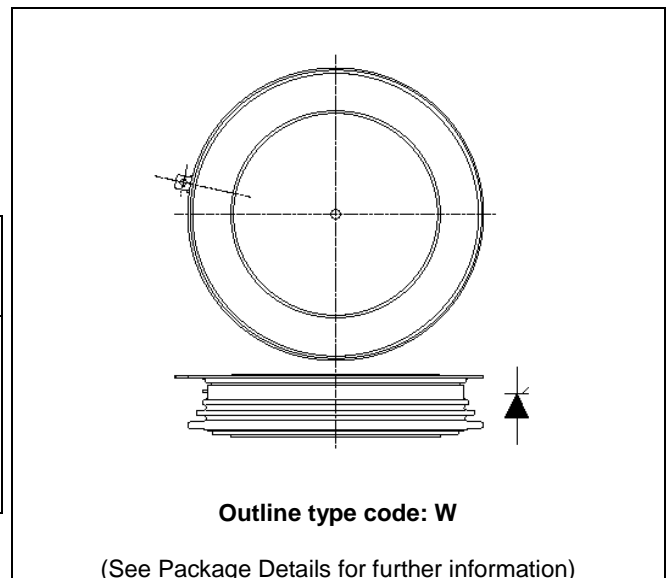


Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR2950W65

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

$T_{case} = 60^{\circ} C$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2945	A
$I_{T(RMS)}$	RMS value	-	4629	A
I_T	Continuous (direct) on-state current	-	4430	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ} C$	38.85	kA
I^2t	I^2t for fusing	$V_R = 0$	7.55	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00631	$^{\circ} C/W$
		Single side cooled	Anode DC	-	0.01115	$^{\circ} C/W$
			Cathode DC	-	0.01453	$^{\circ} C/W$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 76.0kN (with mounting compound)	Double side	-	0.0014	$^{\circ} C/W$
			Single side	-	0.0028	$^{\circ} C/W$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}	-	125	$^{\circ} C$	
T_{stg}	Storage temperature range		-55	125	$^{\circ} C$	
F_m	Clamping force		68.0	84.0	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	300	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	1500	V/ μ s	
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$	Repetitive 50Hz	-	150	A/ μ s
		Gate source 30V, 10 Ω , $t_r < 0.5\mu$ s, $T_j = 125^{\circ}C$	Non-repetitive	-	300	A/ μ s
$V_{T(TO)}$	Threshold voltage – Low level	500 to 2400A at $T_{case} = 125^{\circ}C$	-	0.94	V	
	Threshold voltage – High level	2400 to 7200A at $T_{case} = 125^{\circ}C$	-	1.13	V	
r_T	On-state slope resistance – Low level	500A to 2400A at $T_{case} = 125^{\circ}C$	-	0.343	m Ω	
	On-state slope resistance – High level	2400A to 7200A at $T_{case} = 125^{\circ}C$	-	0.264	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu$ s, $T_j = 25^{\circ}C$	-	3	μ s	
t_q	Turn-off time	$T_j = 125^{\circ}C$, $V_R = 200V$, dI/dt = 1A/ μ s, dV _{DR} /dt = 20V/ μ s linear	-	1200	μ s	
Q_S	Stored charge	$I_T = 2000A$, $T_j = 125^{\circ}C$, dI/dt – 1A/ μ s,	2800	6400	μ C	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	-	3	A	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	-	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25° C	1.5	V
V _{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25° C	250	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	15	mA

CURVES

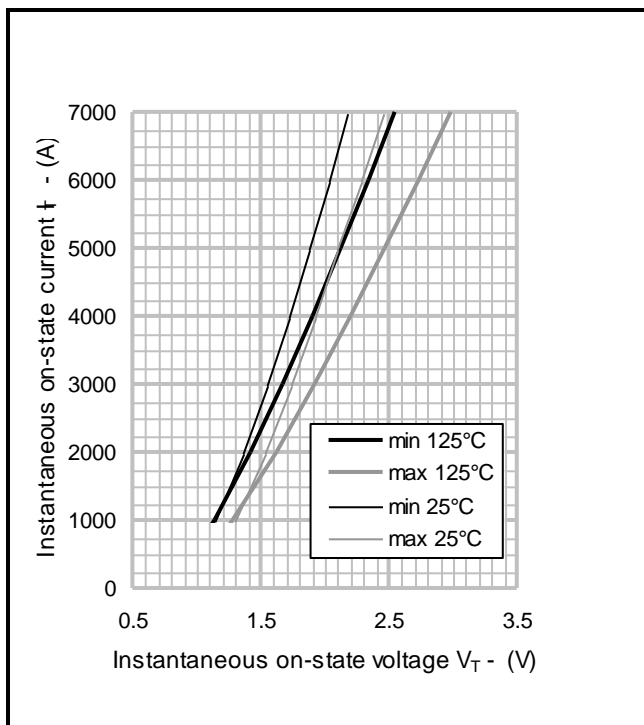


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.914146
 B = -0.3808
 C = 0.00016
 D = 0.015311

these values are valid for T_j = 125° C for I_T 500A to 7200A

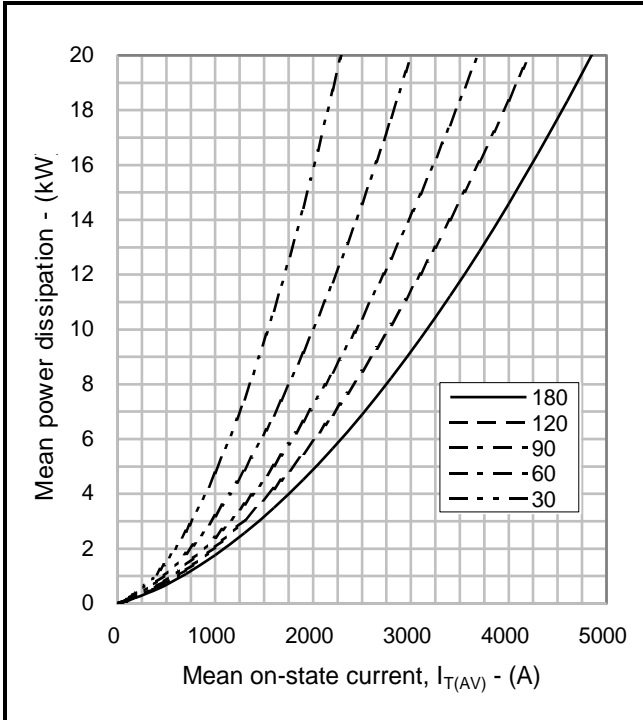


Fig.3 On-state power dissipation – sine wave

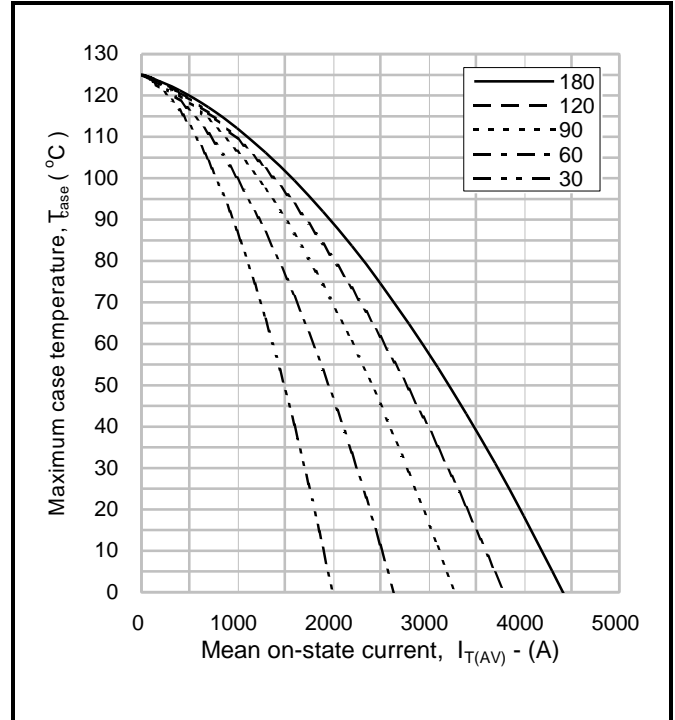


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

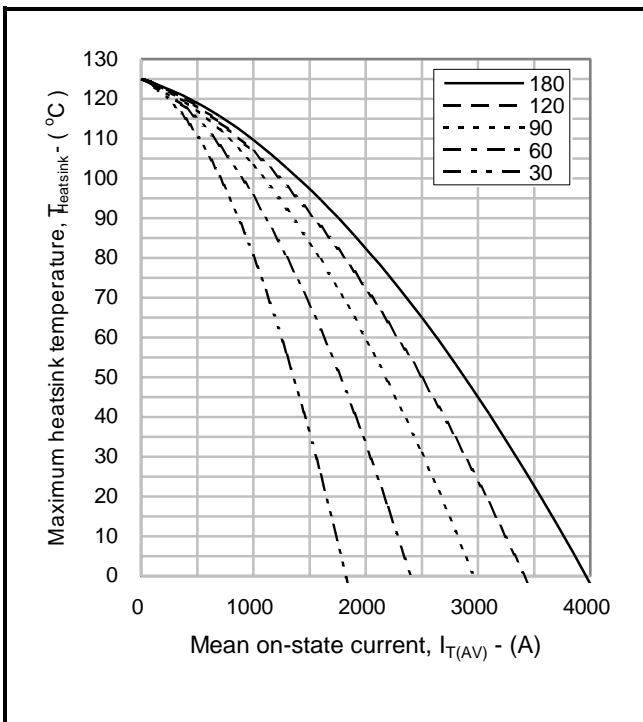


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

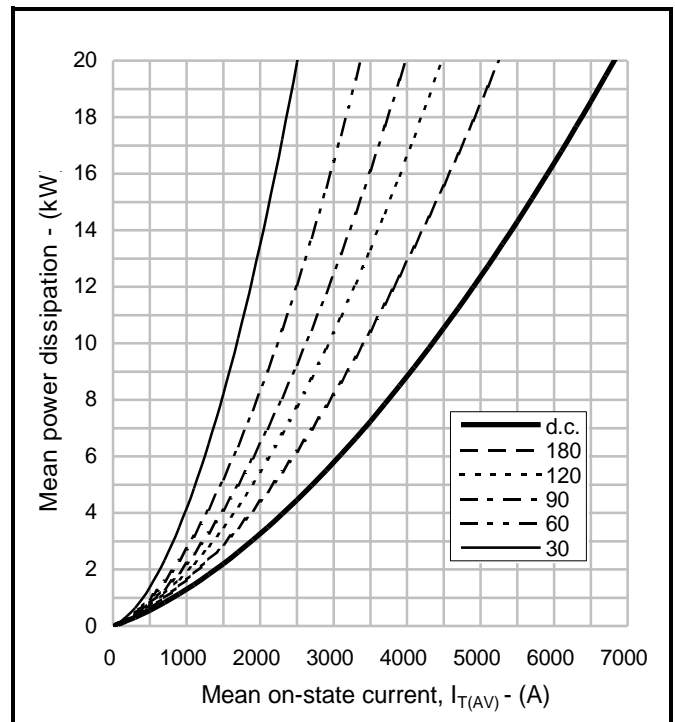


Fig.6 On-state power dissipation – rectangular wave

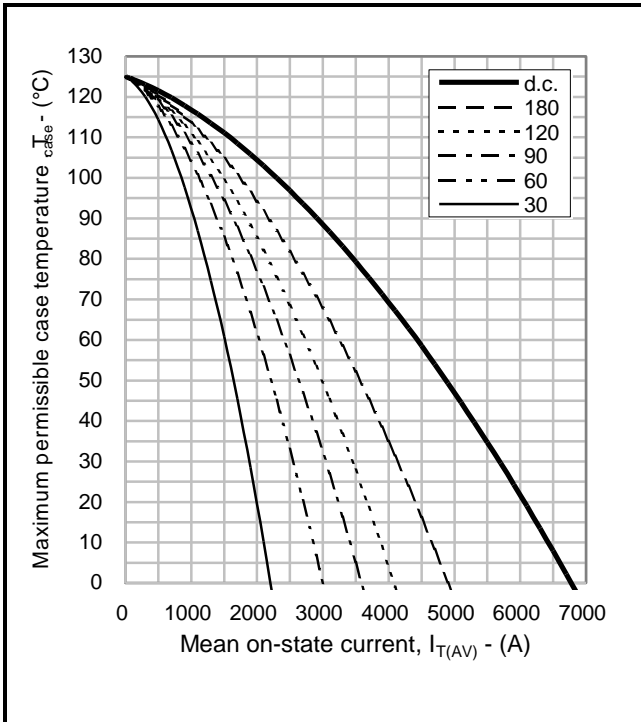


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

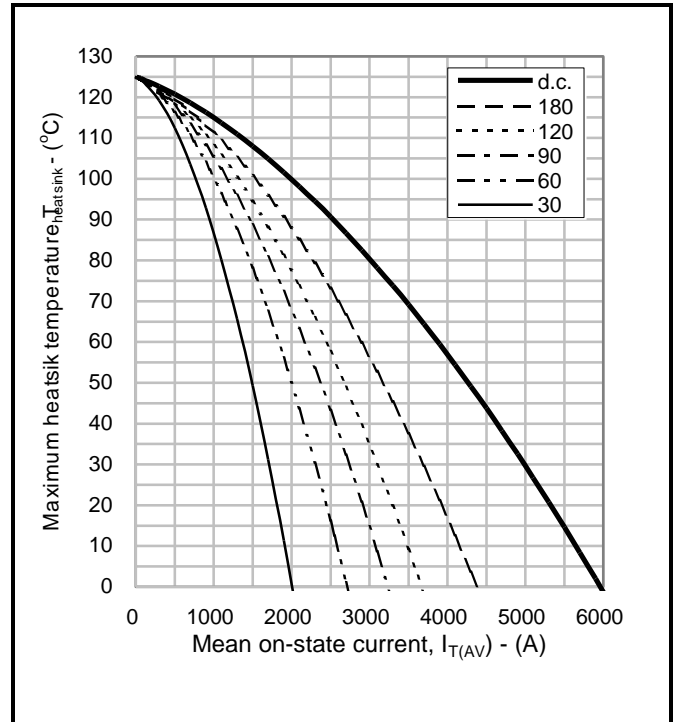


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

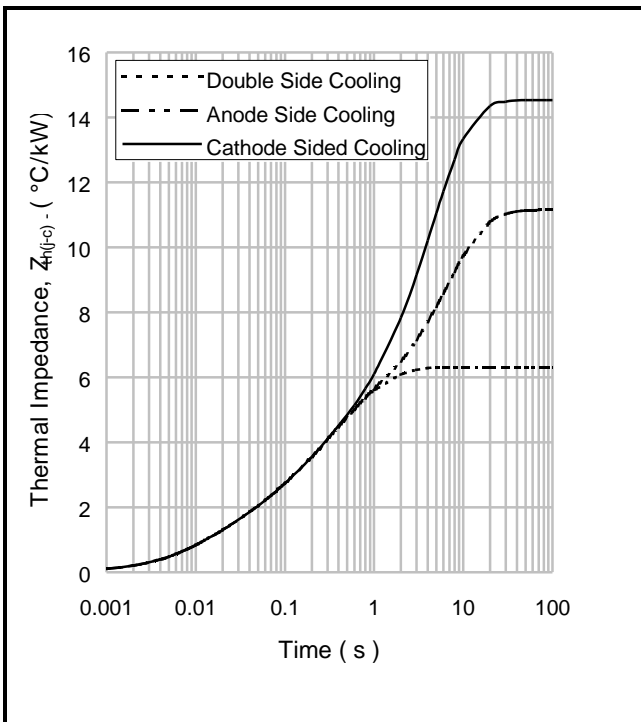


Fig.9 Maximum (limit) transient thermal impedance – junction to case (° C/kW)

		1	2	3	4
Double side cooled	R_{θ} (°C/kW)	0.8816	1.2993	2.8048	1.3305
	T_1 (s)	0.0106818	0.058404	0.3584979	1.1285
Anode side cooled	R_{θ} (°C/kW)	1.5197	3.2398	5.7622	0.6312
	T_1 (s)	0.0170581	0.2424644	6.013	15.364
Cathode side cooled	R_{θ} (°C/kW)	1.4106	2.4667	6.7451	3.9054
	T_1 (s)	0.0158344	0.1786951	3.6201	6.196

$$Z_{th} = \sum [R_i \times (1 - \exp. (-t/t_i))] \quad [1]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
ρ°	$\Delta Z_{th} (z)$		ρ°	$\Delta Z_{th} (z)$		ρ°	$\Delta Z_{th} (z)$	
	sine.	rect.		sine.	rect.		sine.	rect.
180	1.00	0.67	180	0.94	0.64	180	0.95	0.65
120	1.16	0.97	120	1.08	0.91	120	1.09	0.92
90	1.33	1.13	90	1.23	1.06	90	1.25	1.07
60	1.48	1.31	60	1.37	1.22	60	1.38	1.23
30	1.61	1.51	30	1.47	1.38	30	1.49	1.40
15	1.66	1.61	15	1.52	1.47	15	1.54	1.49

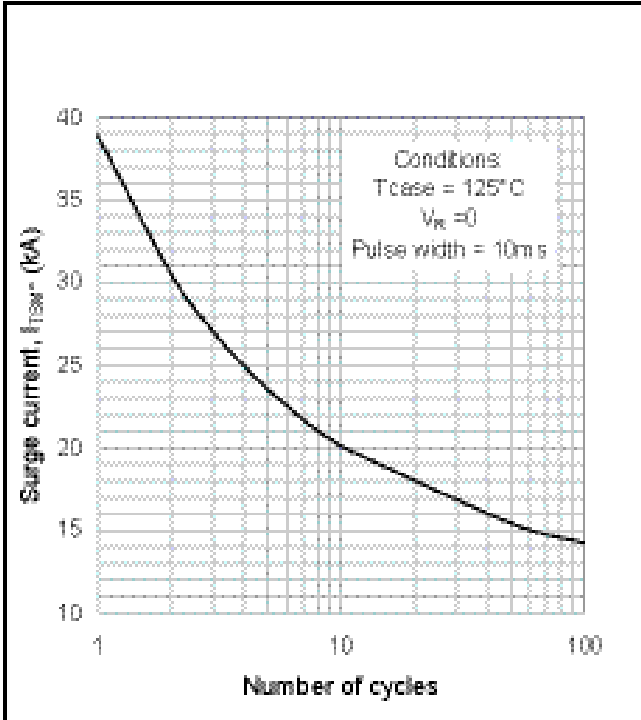


Fig.10 Multi-cycle surge current

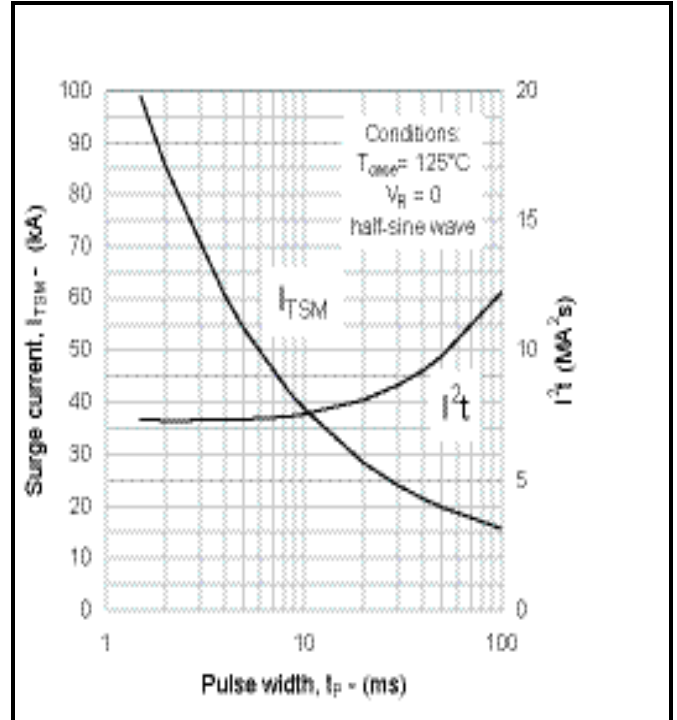


Fig.11 Single-cycle surge current

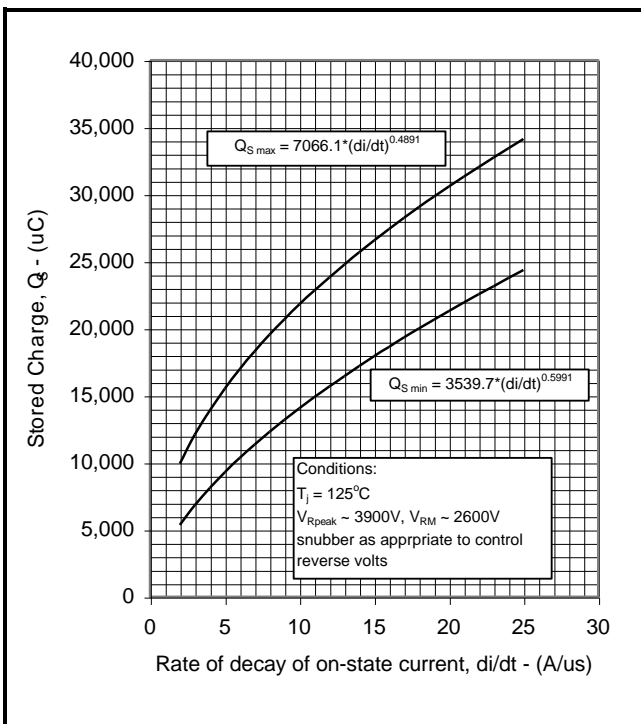


Fig.10 Reverse recovery charge

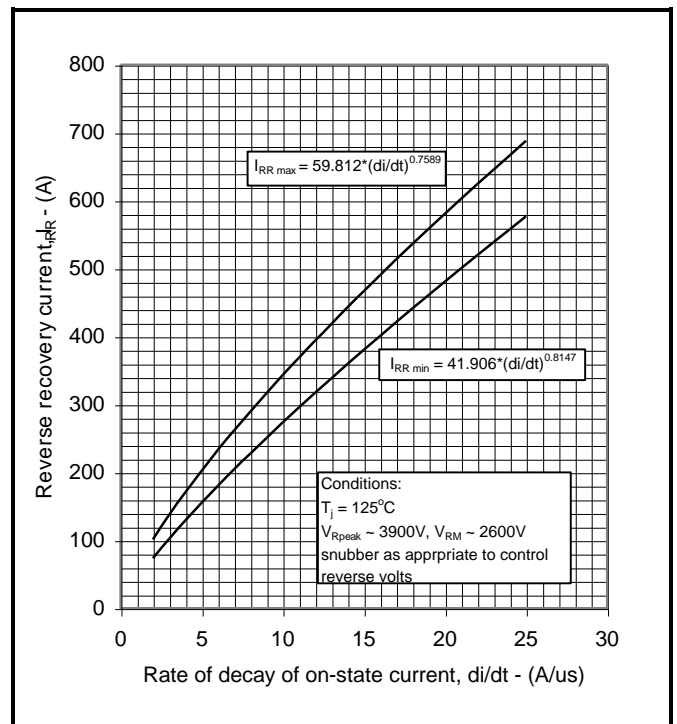


Fig.11 Reverse recovery current

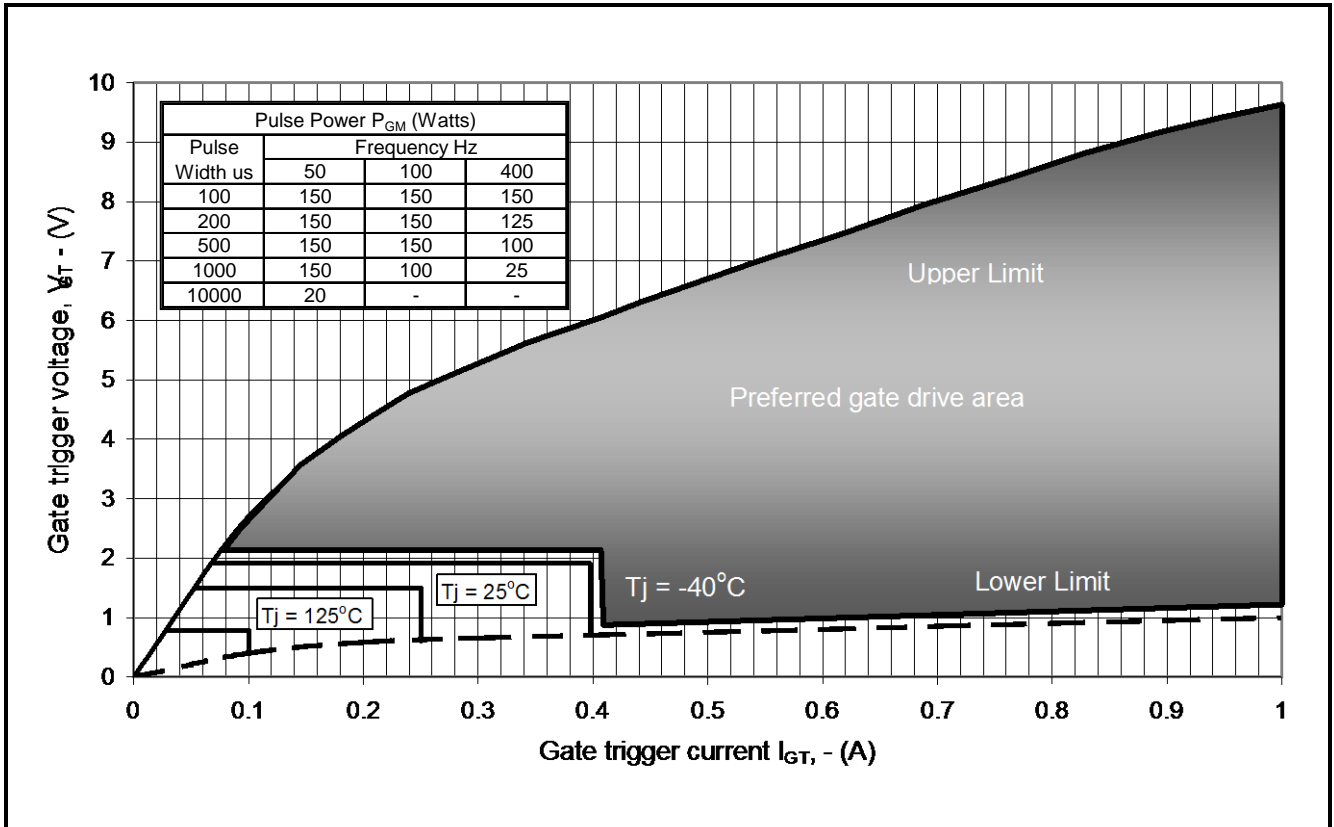


Fig12 Gate Characteristics

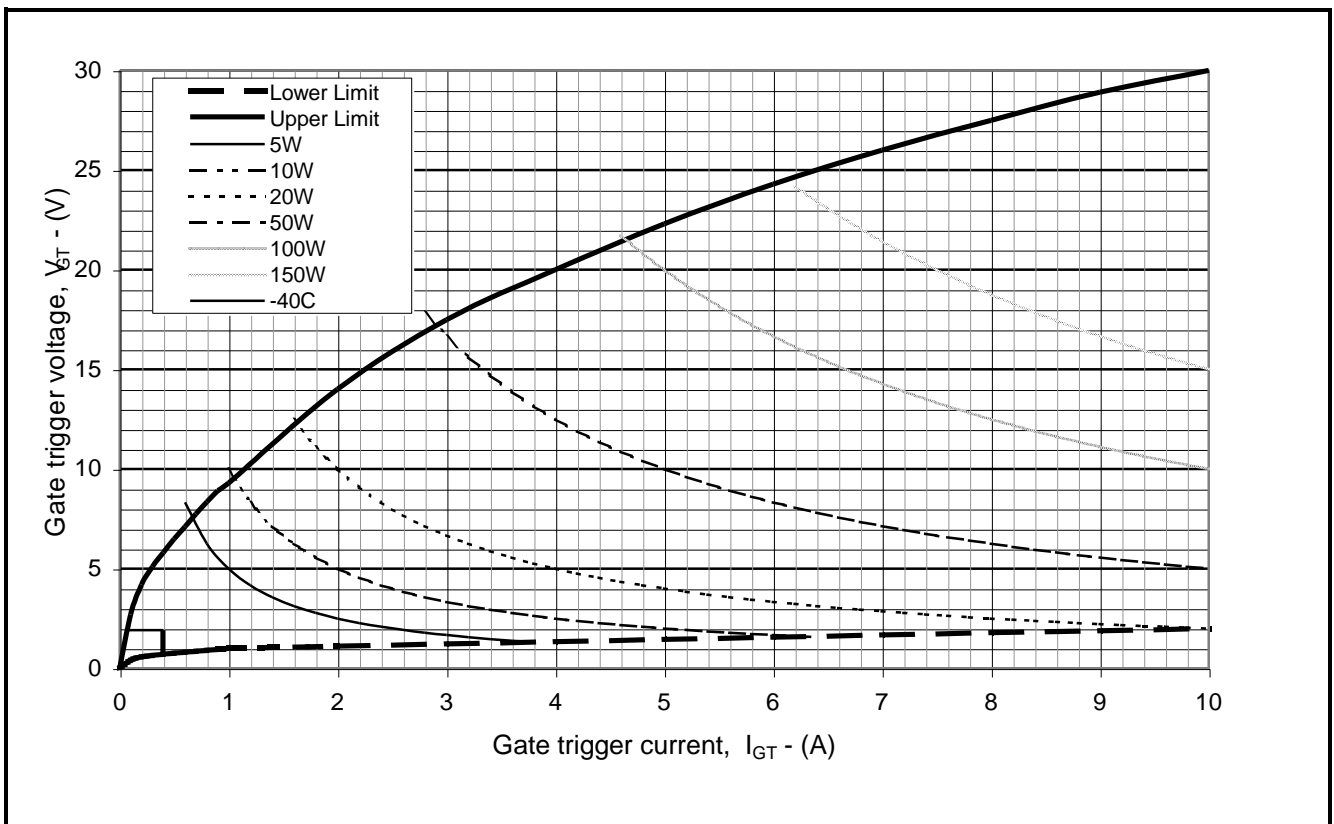


Fig. 13 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. **DO NOT SCALE.**

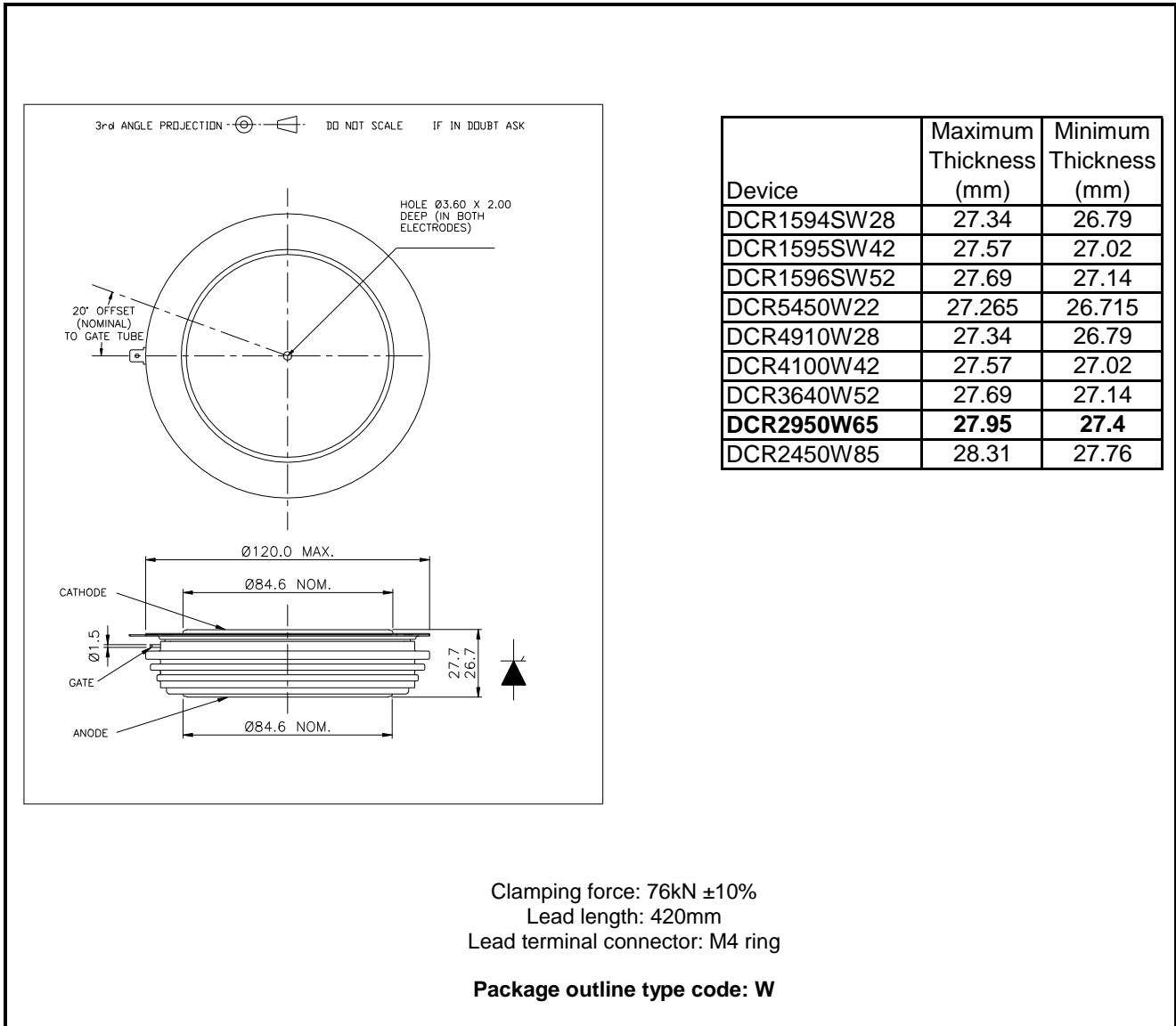


Fig.14 Package outline

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

HEADQUARTERS OPERATIONS

DYNEX SEMICONDUCTOR LIMITED
Doddington Road, Lincoln, Lincolnshire, LN6 3LF
United Kingdom.
Phone: +44 (0) 1522 500500
Fax: +44 (0) 1522 500550
Web: <http://www.dynexsemi.com>

CUSTOMER SERVICE

Phone: +(0) 1522 502753 / 502901
Fax: +(0) 1522 500020
e-mail: power_solutions@dynexsemi.com

© Dynex Semiconductor 2003 TECHNICAL DOCUMENTATION – NOT FOR RESALE. PRODUCED IN UNITED KINGDOM.

This publication is issued to provide information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. The Company reserves the right to alter without prior notice the specification, design or price of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to the Company's conditions of sale, which are available on request.

All brand names and product names used in this publication are trademarks, registered trademarks or trade names of their respective owners.