

Phase Control Thyristor Preliminary Information



DS5803-1.2 August 2007 (LN25541)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR2630C28	2800	$T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 200\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, V_{DSM} & $V_{RSM} =$ V_{DRM} & $V_{RRM} + 100\text{V}$ respectively
DCR2630C26	2600	
DCR2630C24	2400	

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR2630C28

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	2800V
$I_{T(AV)}$	2630A
I_{TSM}	35250A
dV/dt^*	1500V/μs
dI/dt	300A/μs

* Higher dV/dt selections available

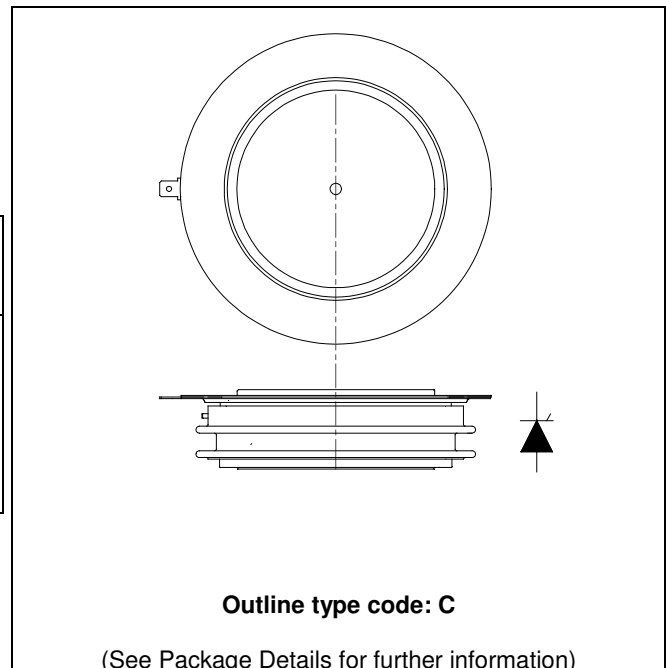


Fig. 1 Package outline

CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2630	A
$I_{T(RMS)}$	RMS value	-	4130	A
I_T	Continuous (direct) on-state current	-	3900	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	35.25	kA
I^2t	I^2t for fusing	$V_R = 0$	6.21	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0101	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.0176	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0239	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 37kN (with mounting compound)	Double side	-	0.0025	$^{\circ}\text{C/W}$
			Single side	-	0.005	$^{\circ}\text{C/W}$
T_{vj}	Virtual junction temperature	On-state (conducting)	-	135	$^{\circ}\text{C}$	
		Reverse (blocking)	-	125	$^{\circ}\text{C}$	
T_{stg}	Storage temperature range		-55	125	$^{\circ}\text{C}$	
F_m	Clamping force		33.0	41.0	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	200	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	1500	V/ μs	
dl/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$	Repetitive 50Hz	-	150	A/ μs
		Gate source 30V, 10 Ω , $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$	Non-repetitive	-	300	A/ μs
$V_{T(TO)}$	Threshold voltage – Low level	500A to 1250A at $T_{case} = 125^{\circ}C$	-	0.817	V	
	Threshold voltage – High level	1250A to 7000A at $T_{case} = 125^{\circ}C$	-	0.974	V	
r_T	On-state slope resistance – Low level	500A to 1250A at $T_{case} = 125^{\circ}C$	-	0.2366	m Ω	
	On-state slope resistance – High level	1250A to 7000A at $T_{case} = 125^{\circ}C$	-	0.1665	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu s$, $T_j = 25^{\circ}C$	TBD	TBD	μs	
t_q	Turn-off time	$T_j = 125^{\circ}C$, $V_R = 200V$, $dl/dt = 1A/\mu s$, $dV_{DR}/dt = 20V/\mu s$ linear	100	250	μs	
Q_S	Stored charge	$I_T = 2000A$, $T_j = 125^{\circ}C$, $dl/dt = 1A/\mu s$,	450	2000	μC	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	-	3	A	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	-	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25°C	1.5	V
V _{GD}	Gate non-trigger voltage	At V _{DRM} , T _{case} = 125°C	TBD	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25°C	250	mA
I _{GD}	Gate non-trigger current	V _{DRM} = 5V, T _{case} = 25°C	TBD	mA

CURVES

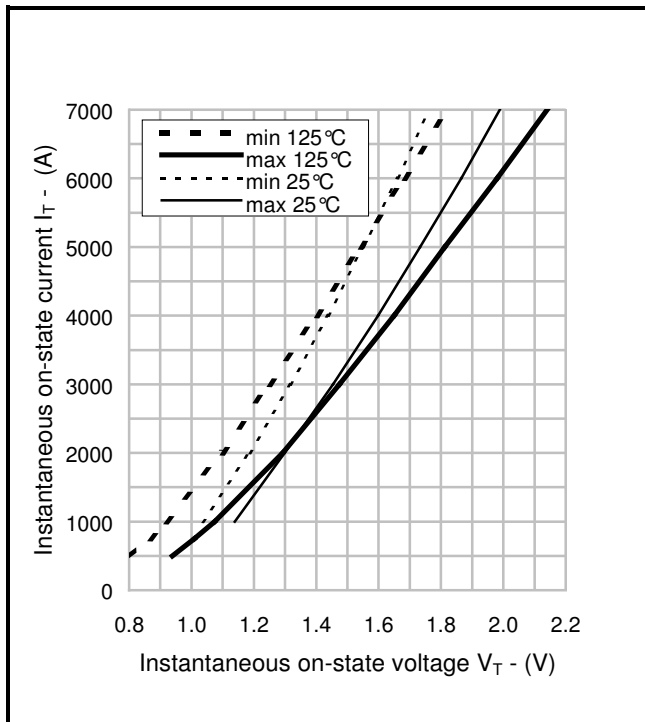


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.508059
 B = 0.643422
 C = 0.000125
 D = 0.004454

these values are valid for T_j = 125°C for I_T 100A to 7200A

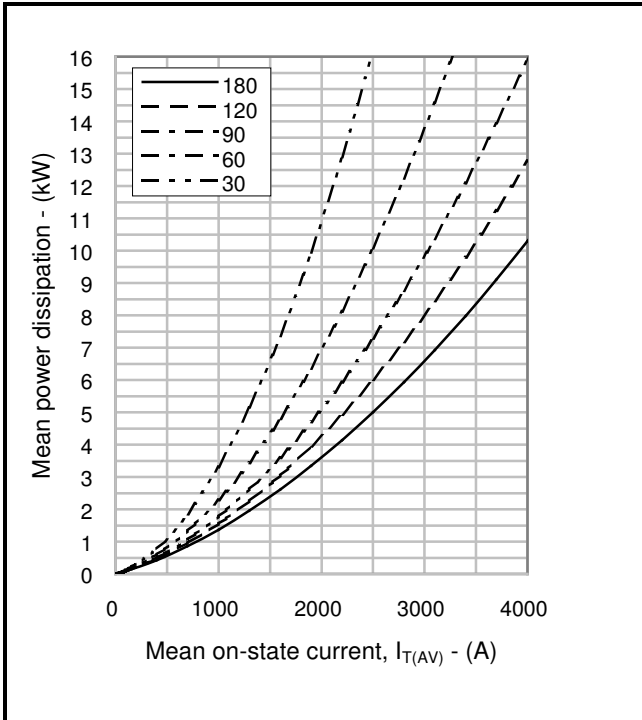


Fig.3 On-state power dissipation – sine wave

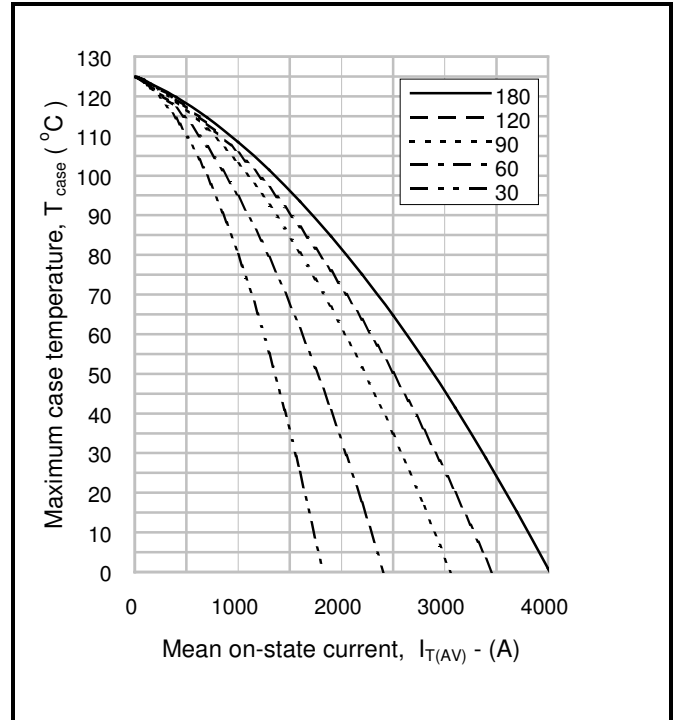


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

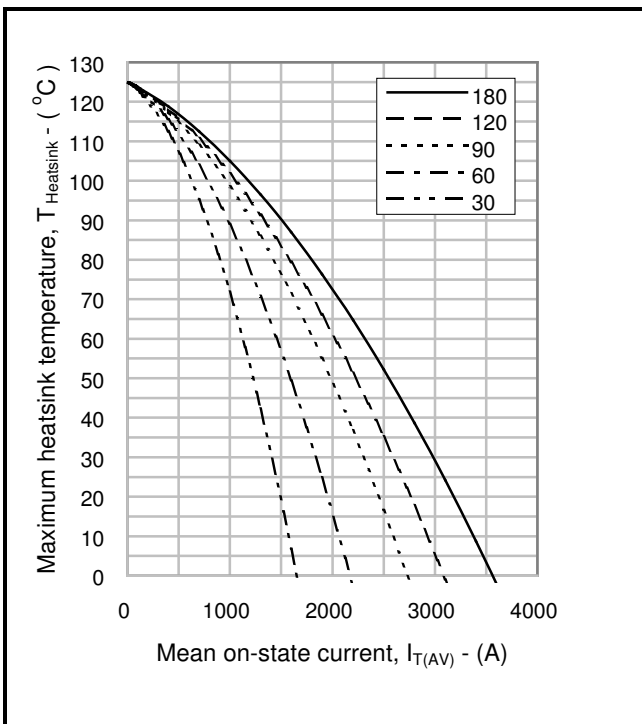


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

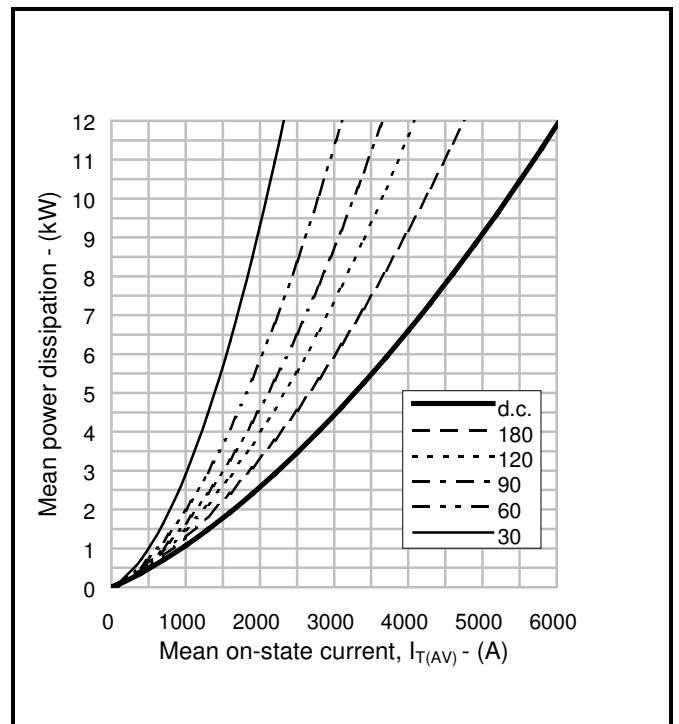


Fig.6 On-state power dissipation – rectangular wave

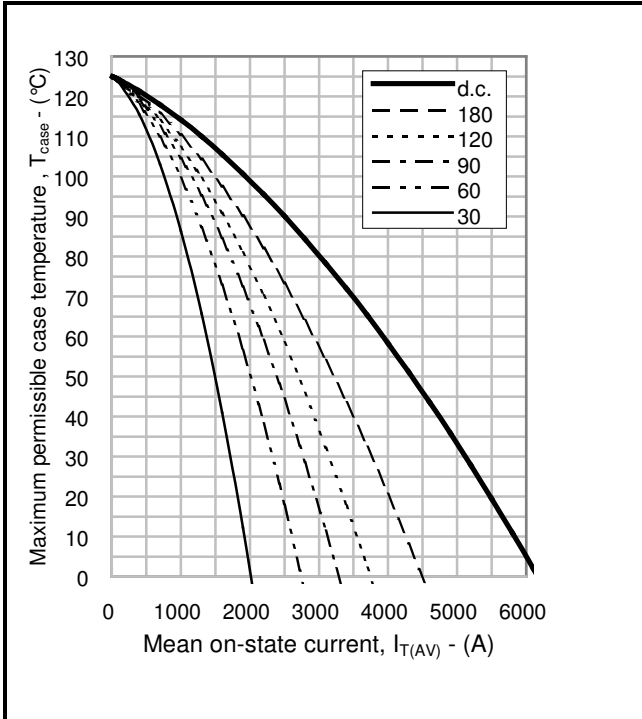


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

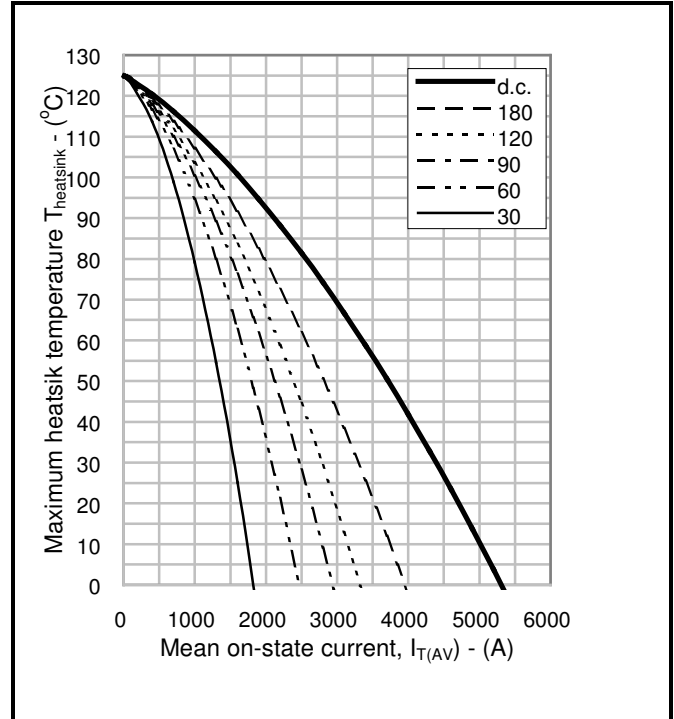


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

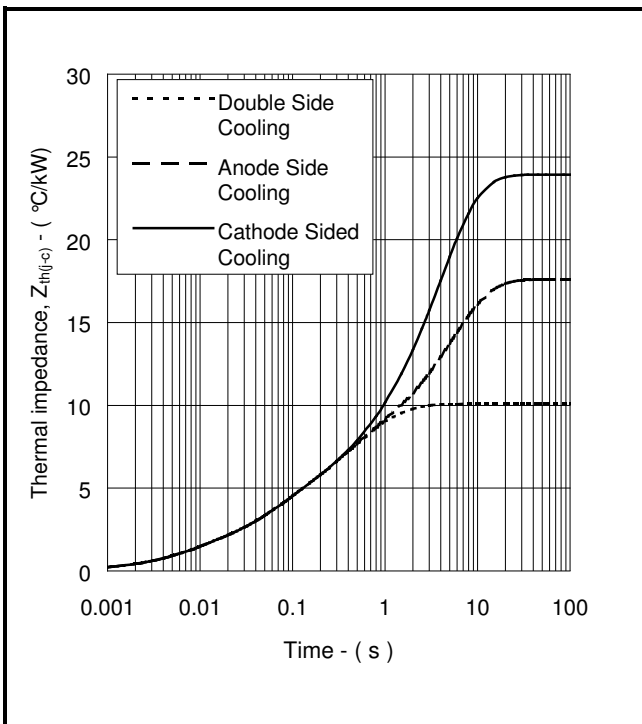


Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

		1	2	3	4
Double side cooled	R _i (°C/kW)	1.1043	2.576	4.5096	1.9009
	T _i (s)	0.006176	0.0517916	0.3820376	1.06
Anode side cooled	R _i (°C/kW)	1.0977	2.4566	4.0469	9.9994
	T _i (s)	0.006153	0.050142	0.3129407	5.27
Cathode side cooled	R _i (°C/kW)	1.1519	2.8926	2.4064	17.4793
	T _i (s)	0.006389	0.0582953	0.3775516	3.97

$$Z_{th} = \sum [R_i \times (1 - \exp. -(t/t_i))] \quad [1]$$

ΔR_{th(j-c)} Conduction

Tables show the increments of thermal resistance R_{th(j-c)} when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
α°	ΔZ _{th} (z)		α°	ΔZ _{th} (z)		α°	ΔZ _{th} (z)	
	sine.	rect.		sine.	rect.		sine.	rect.
180	1.95	1.26	180	1.95	1.26	180	1.95	1.26
120	2.32	1.89	120	2.32	1.89	120	2.31	1.88
90	2.74	2.27	90	2.74	2.27	90	2.72	2.26
60	3.14	2.70	60	3.14	2.70	60	3.12	2.68
30	3.46	3.19	30	3.46	3.19	30	3.43	3.17
15	3.61	3.47	15	3.62	3.47	15	3.58	3.44

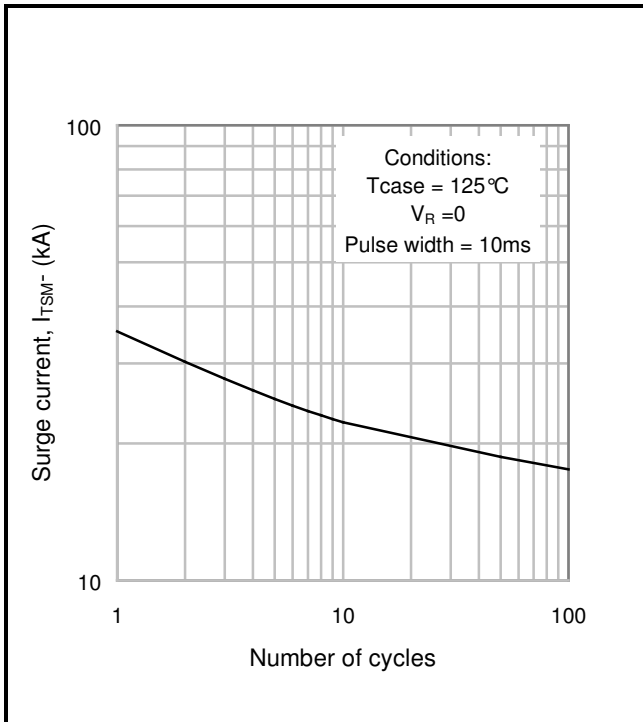


Fig.10 Multi-cycle surge current

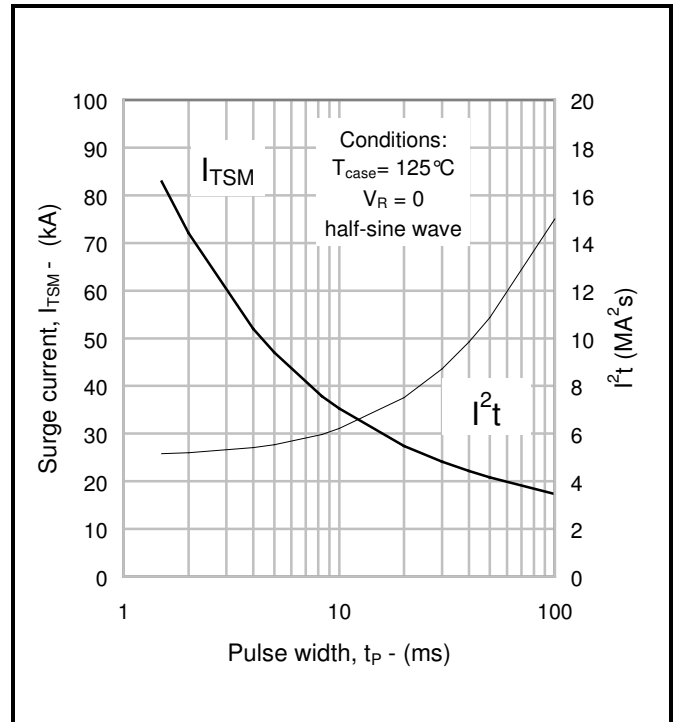


Fig.11 Single-cycle surge current

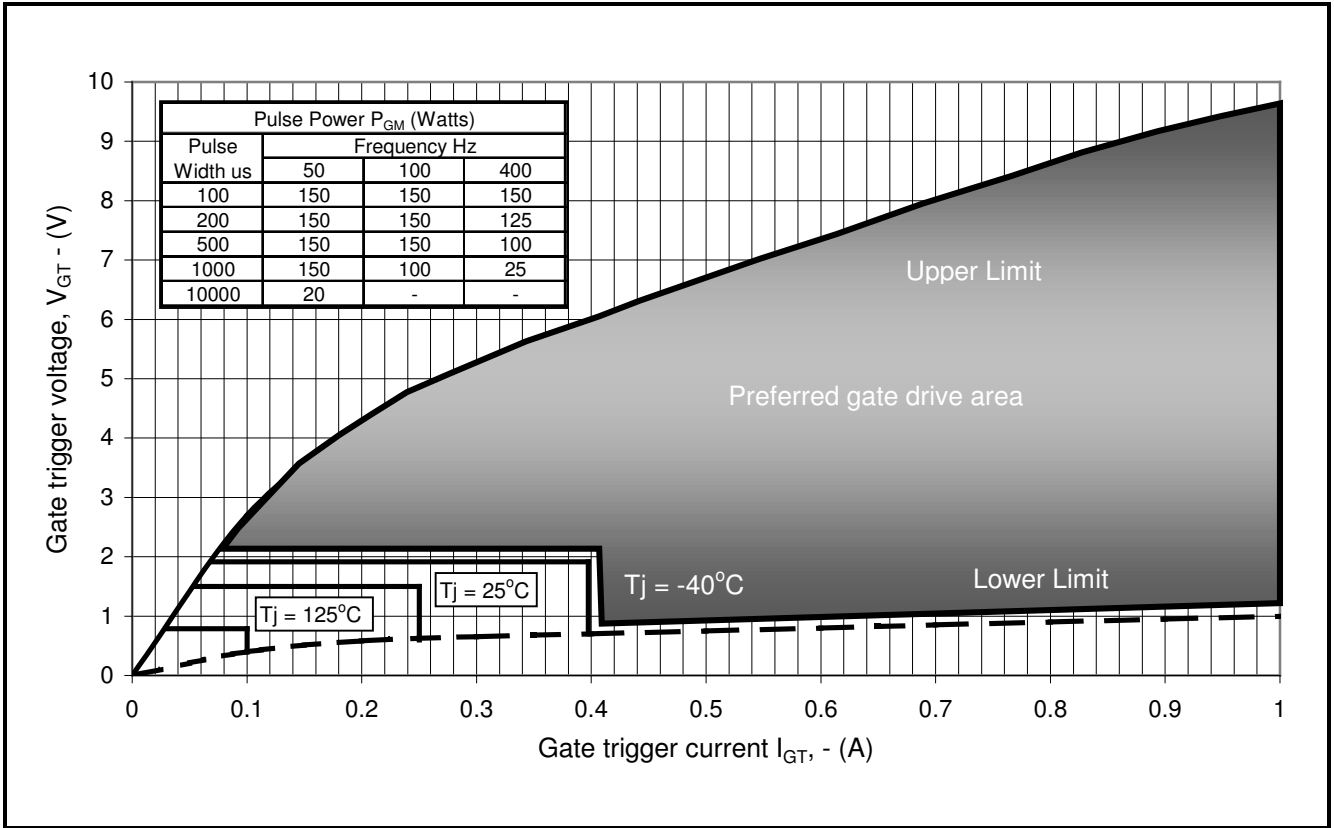


Fig12 Gate Characteristics

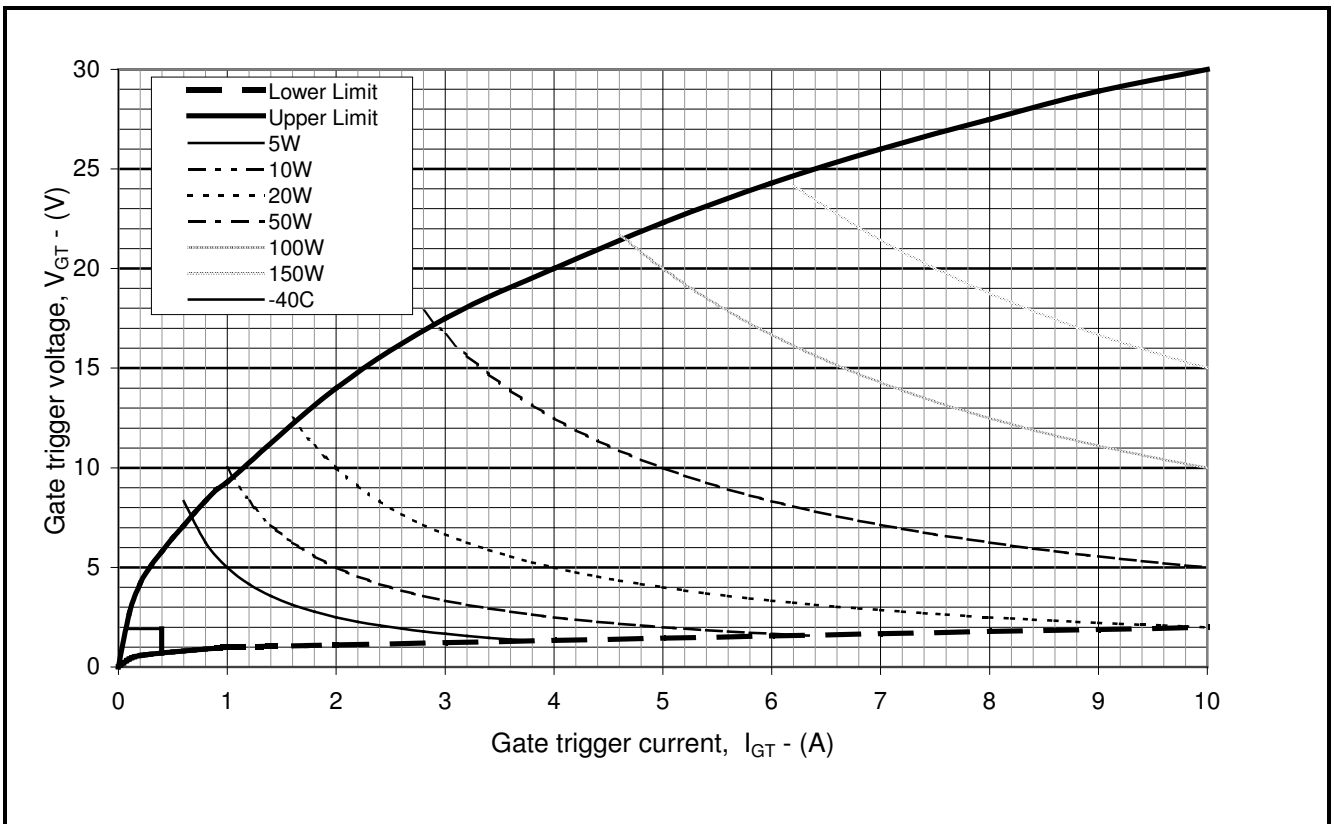


Fig. 13 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

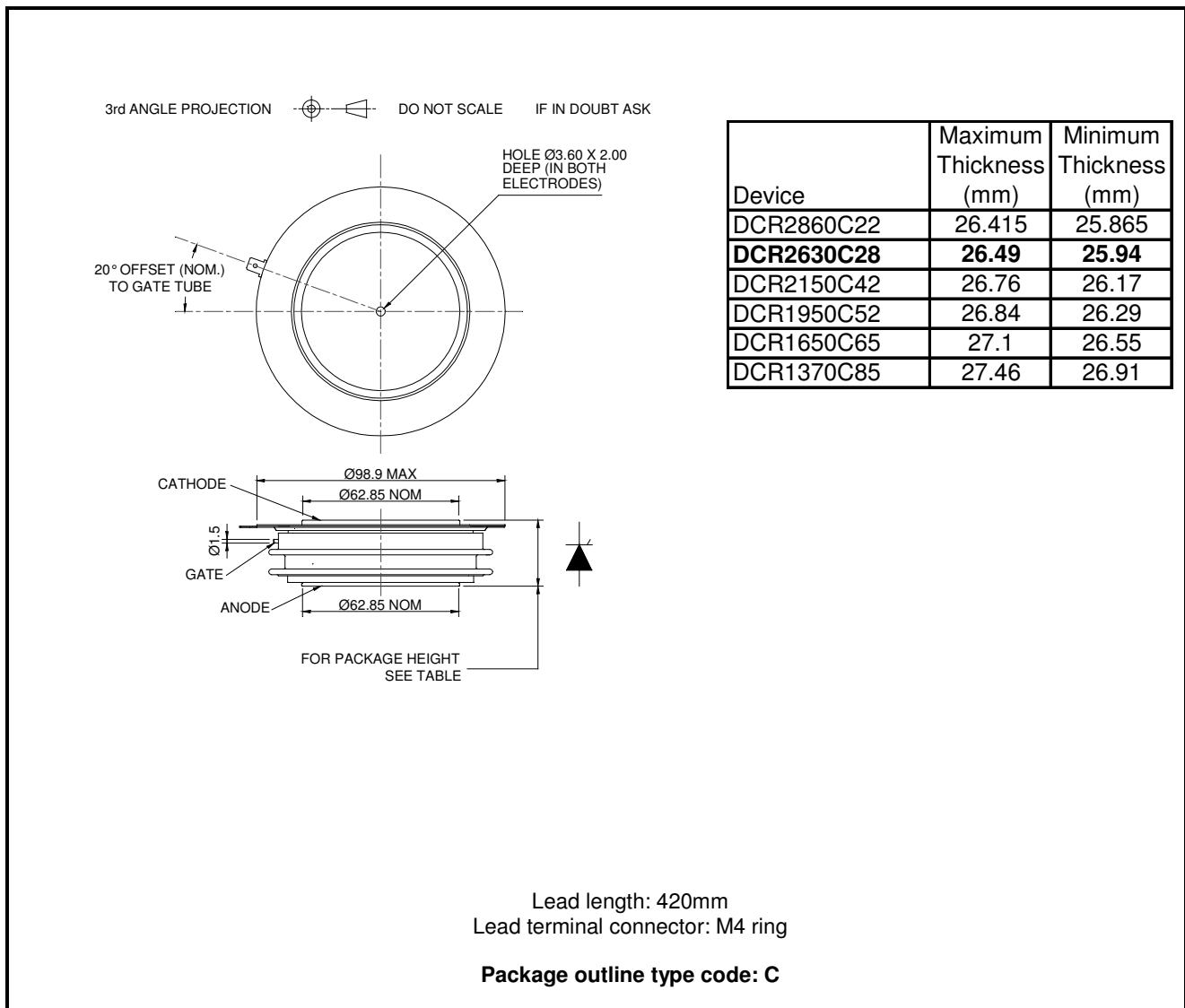


Fig.14 Package outline

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



<http://www.dynexsemi.com>

e-mail: power_solutions@dynexsemi.com

**HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LTD**
Doddington Road, Lincoln
Lincolnshire, LN6 3LF. United Kingdom.
Tel: +44(0)1522 500500
Fax: +44(0)1522 500550

CUSTOMER SERVICE
Tel: +44(0)1522 502753 / 502901. Fax: +44(0)1522 500020

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