Exploring the RBSOA Boundaries of a 6.5kV/1000A Trench Gate IGBT Module at Different Temperatures

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The Power Point Presentation will be available after the conference.

Abstract

Under fault conditions especially in HVDC applications, IGBT modules in a series or parallel configuration may have to withstand very high line voltages(Vline) and still expected to turn-off safely. Under such extreme conditions the devices are usually operating outside their datasheet recommended RBSOA where turn-off can be limited by increased dynamic avalanche, which increases turn-off energy loss (E_{off}). Excessive E_{off} impacts reliability by accelerating wear out and increase the likelyhood of thermal runaway and device destruction. In this paper, we explore Dynex's 6.5kV/1000A Trench gate IGBT module RBSOA at extremely high voltages and at different temperatures. Based on experimental results and simulation study, some recommendatons for improvements are proposed, regarding device design to reduce dynamic avalanche and time under SSCM (Switching Self-Clamping Mode).

1. Introduction

During PCIM'19 Dynex presented its new 6.5kV/1000A IGBT module variants suitable for HVDC and traction type applications in the 190mmx140mm footprint (Fig.1) [1]. Traditionally a 6.5kV IGBT module datasheet RBSOA curve is obtained by switching typically 2xInom at for example Vce=4.5kV to leave sufficent room for the overshoot voltage due to stray inductance, not to cause Vce to exceed the breakdown voltage [2-5]. However, under fault conditions an IGBT module in series or parallel configuration may have to withstand Vce > 4.5kV across its terminials and still expected to turn-off safely without exceeding the thermal limits of the package. In this paper for the first time, we show results for high line voltage RBSOA performance of Dynex's 6.5kV/1000A Trench gate IGBT.

The approach is to evaluate the influence of dynamic avalanche on turn-off behaviour and E_{off}, for increasing line voltages up to 5.3kV, whilst keeping turn-off current fixed at 1000A. It is shown that up to Vline=5.3kV, the device turns off safely, the breakdown voltage is not reached and dynamic avalanche dominated SSCM (Switching Self-Clamping Mode) which leads to increased turn-off delay and energy loss, reduces with increasing temperature. Morevover, some optmisation in buffer/collector design and n-base resistivity are shown to reduce the duration of the SSCM period even further in a new device design.

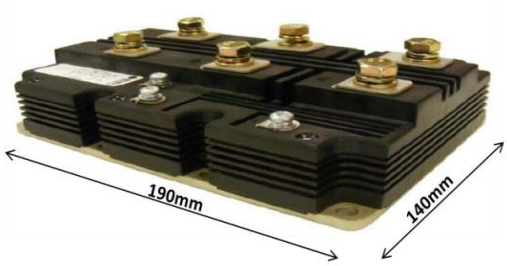

Fig.1: Device under test: The 6.5kV/1000A Trench gate IGBT module in the 190mm x 140mm footprint.

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2. Experimental Results

The RBSOA test set up shown in Fig.2 was used in this work. DUT is a variant of Dynex's low loss 1kA/6.5kV module. Fig.3 shows succesful Ice=2kA turn-off at Vline=4.6kV with peak power ~10MW. So there is sufficient margin for target applications where Vline is typically 3600V. However, the focus of this paper is to explore the RBSOA at Vline > 4.5kV at different temperatures.

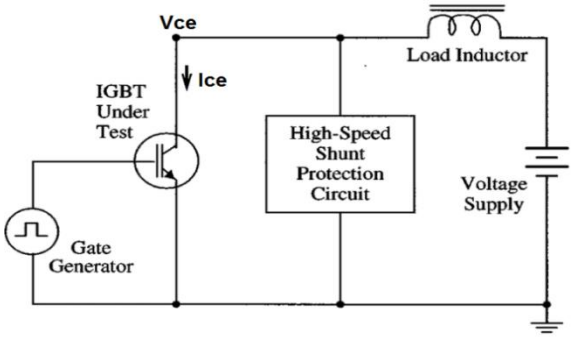


Fig.2: Test circuit for analysis of IGBT Turn-off. The DUT(Device Under Test) is unclamped.

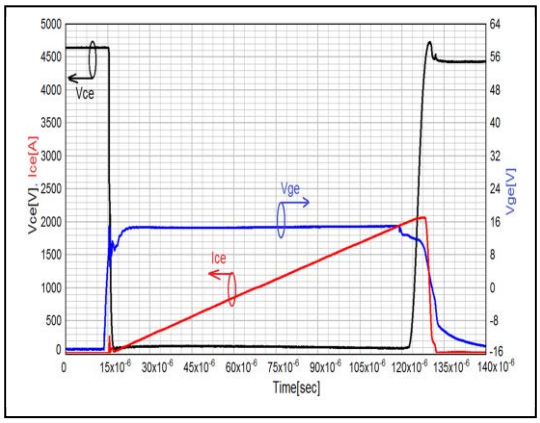
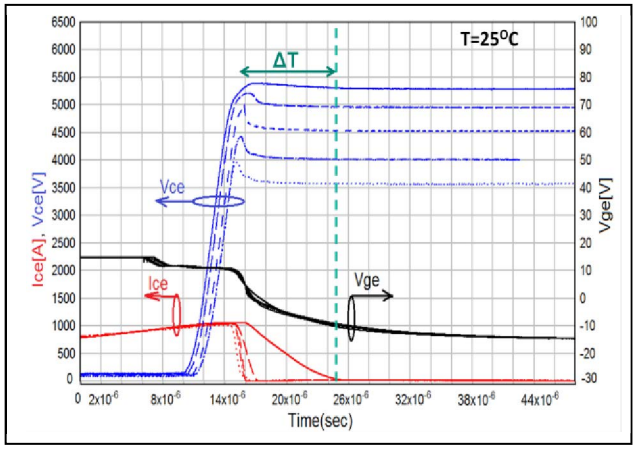
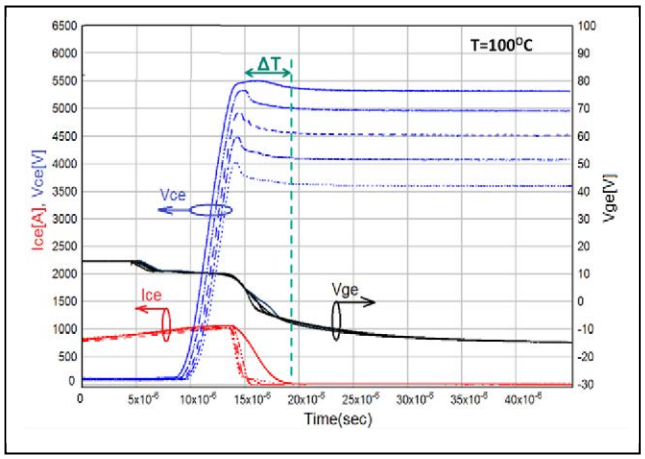


Fig.3: Measured successful Ice=2000A turn-off at Vline=4600V, T=150^{0}C, Vge=±15V, Cge=330nF, R_{goff}=15Ω, Ls=200nH

It is a well known fact that close to the breakdown voltage, the turn-off current for any IGBT module reduces with voltage, So to prevent thermal run-away, switching current is set to 1000A in this work. Fig.4a-b shows succesfull turn-off up to Vline=5.3kV at both 25C and 100^{0}C with peak voltage reaching 5.5kV. In addition, the duration over which the device is under dynamic avalanche dominated



(a)



(b)

Fig.4a-b: Measured waveforms for increasing line voltage turn-off at **a)** 25^{0}C, **b)** 100^{0}C. ΔT is the increase in turn-off delay time due to avalanche SSCM period at 5.3kV. Vline=3.6kV to 5.3kV, Vge=±15V, I_{OFF}=1000A, Ls=200nH, Cge=330nF, R_{goff} =15Ω

SSCM, ΔT, is about 5µs at 100^{0}C compared to ~9.0µs at 25^{0}C. Extended SSCM period at 25^{0}C can lead to excessive E_{off}. The IGBT module is unclamped in the test which means the junction temperature can easliy exceed recommended T_{jmax} in some areas of the module and cause failure, Hence testing was limited to 100^{0}C baseplate temperature.This is supported by device simulation. Device simulation results in Fig.5 shows succesfull 1000A turn-off at 5500V and turn-off failure at 5700V. Also it can be seen that temprature within the failed device keeps on rising which will result in destruction. So even though the baseplate temperature was held at 125^{0}C, only

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a temperature rise of 26^{0}C due to increased E_{off} by dynamic avalanche will make T_{Jmax} larger than the recommended 150^{0}C and cause failure.

During IGBT turn-off and Vce start rising, dynamic avalance begins as soon as the MOS channels supplying electrons to the n-drift region are turned off. Lack of electrons to compensate the recovering holes will modify the effective background doping and the electri field distribution, characterised by lower dV/dt dominated by dynamic avalanche. Unless device failure occurs, dynamic avlanche will continue until the remaining plasma is used up. If the thermal limit is not exceeded, Vce will rise due to stray inductance in the commutation circuit, untill Vce eventually gets close to the device breakdown voltage [6].

The increased current tail at 5.3kV test is because the carriers generated during dynamic avalanche provide additional base current for bipolar pnp action to continue even though the MOS channels are off. So extended SCCM periods can lead to loss of gate control resulting in formation of filaments, temperature rise and device failure.

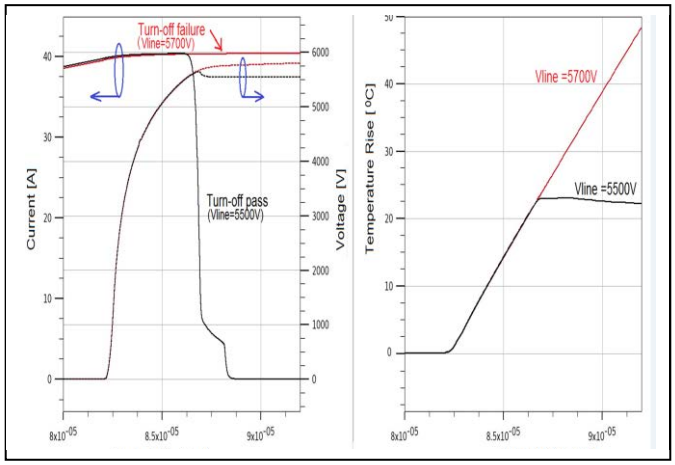

Fig.5: Electro-thermal simulation with baseplate temp=125^{0}C showing successful turn-off at Vline=5500V and failure at 5700V. Whilst the device temperatures start reducing after successful turn-off, it keeps increasing with failure.

3. Optimisations for improved dynamic avalanche performance

During IGBT turn-off when the MOS channels are off, the 1-D electric field course can be described by eq1, if R_{goff} is small enough to have no influence. Hence, the electric field gradient (dE/dx) depends on the doping concentration of the N-base (N_D) and hole density (ρ). Eq2, shows that the current density (J_p) within the device strongly influences dE/dx.

$$\frac{dE}{dx} = \frac{q}{\varepsilon}(N_D + \rho) \qquad \text{Eq1}$$

$$\rho = \frac{J_p}{V_{sat} * q} \qquad \text{Eq2}$$

This means for the same Vce during turn-off a device with higher plasma density (or current density) will have higher dE/dx (and higher electric field) due to smaller space charge, because the depletion edge progresses much slower towards the collector junction. High electric field means increased impact ionization hence dynamic avalanche

3.1 Buffer and Collector design

Fig.6 shows simulated influence of different buffer and collector designs on IGBT turn-off performance. The reference is an ideal case of the standard structure (A), where the impact ionization(II) switch which models dynamic avalanche is turned-off. It can be seen that low collector(C), buffer with lifetime-control or LC buffer (B) and a combination of low collector and deep buffer (D) designs can improve dynamic avalanche performance but at the expense of Vce(sat) as shown in table-1. The onset of dynamic avalanche is shown by A', B', C' and D' arrows indicating points where the Vce slope become less than that of the reference Vce(ref).

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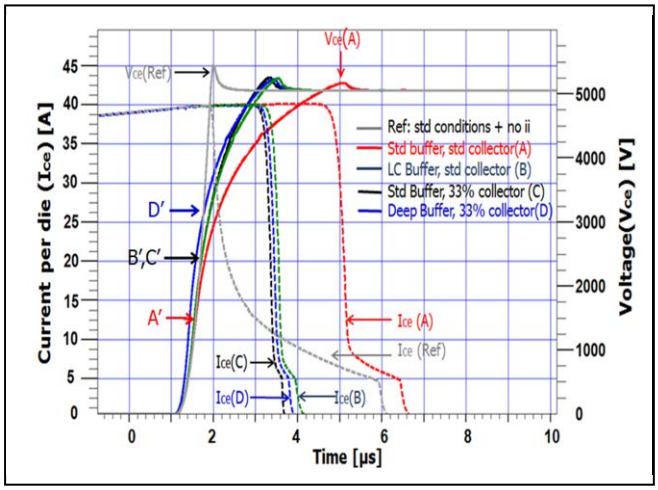

Fig.6: Simulated turn-off Ice and Vce waveforms for different buffer and collector designs (A-D) compared with ideal case of standard structure where impact ionization is turned off. Arrows A-D indicates the onset of dynamic avalanche, when Vce slope becomes less than that of Vce(ref). Vline=5kV, Ice=42A, R_{goff}=8Ω, T=25^{0}C

Table1: Simulated influence of different buffer an collector designs on dynamic avalanche, Vce(sat and Eoff performance. Vce=5kV, Ice=42A, R_{goff} =8Ω, T=25^{0}C

Simulated structure	Buffer Design	Collector Design	Impact ionization (ii)	Onset of Dynamic Avalanche [V]	Vce(sat) [V]	E_{off} per die [J]
Ref	std	std	OFF	ref	2.4	0.29(ref)
A	std	std	ON	1500	2.4	0.64 (+120%)
B	LC	std	ON	2500	3.1	0.35(+20%)
C	std	33%	ON	2500	3.5	0.31(+7%)
D	66% Dose + Extended depth	33%	ON	3200	3.2	0.35(+20%)

It shows that although structures B, C, and D improve dynamic avalanche performance due to reduced hole injection and plasma density within the device, low dose deep buffer structure D, improves the onset of dynamic avalanche to Vce=3200V compared to 2500V in B and C and only 1500V in A.

3.2 Influence of N-base resistivity

From eq2, higher n-base resistivity (i.e. smaller N_D) results in lower dE/dx. Other benefits of smaller N_D include higher breakdown voltage and reduced FIT rates due to lower peak electric field. Fig.7 shows that increased silicon resistivity can improve dynamic avalanche performance as dV/dt gets faster, turn-off delay reduced, and current tail becomes smaller. The simulated E_{off} reduction is 7% and 15% respectively for 125% and 150% resistivity structures. Another benefit of increased silicon resistivity is that Vce(sat) is not compromised due to conductivity modulation of the IGBT n-base due to bipolar action. However sufficient consideration must be given to the choice of silicon resistivity as very low N-base doping may lead to thermal effects such as easy formation of filaments at high temperatures.

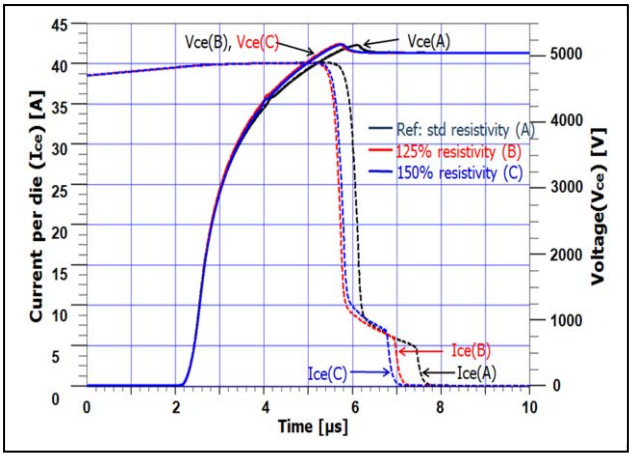

Fig7: Simulated turn-off Ice and Vce waveforms for different n-base resistivity

4. Performance of new optimised device

A new optmised IGBT device has been created taking into consideration some of the features discussed above in addition to top cell modifications. At 1000A, the module shows Vce(sat) of 2.3V and 2.8V at 25^{0}C and 150^{0}C respectively. Fig.8a and b shows measured waveforms where compared to Fig4, the duration of SSCM, at Vline=5.3kV has decreased from 9µs to 4µs at 25^{0}C and from 5us to 2us at 100^{0}C. This results in significant E_{off} reduction at 5.3kV, of between 40-50%, as shown in Fig.9. The new design improves, the point Vline-E_{off} linearity is lost due to avalanche domination, from 4.5kV to 5.2kV at 25^{0}C, while at 100^{0}C, from 5.0kV to >5.4kV.

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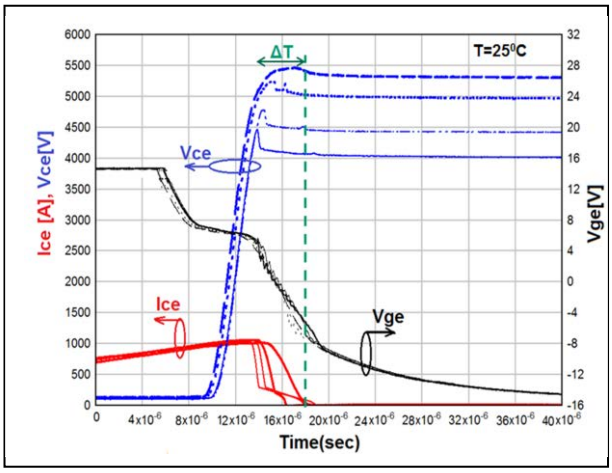
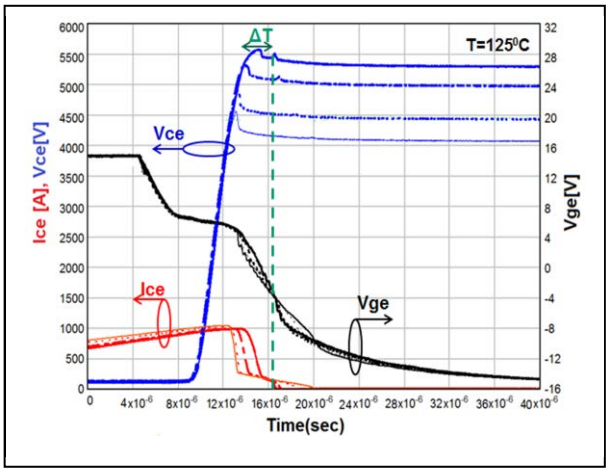


(a)



(b)

Fig.8a-b: Measured waveforms of optimised module for increasing Vline turn-off at **a)** 25^0C and **b)** 100^0C. ΔT is the increase in turn-off delay time due to avalanche SSCM period at 5.3kV. Vline=3.6-5.3kV, Vg=±15V, I_{OFF}=1000A, Ls=200nH, Cge=330nF, R_{goff} =15Ω

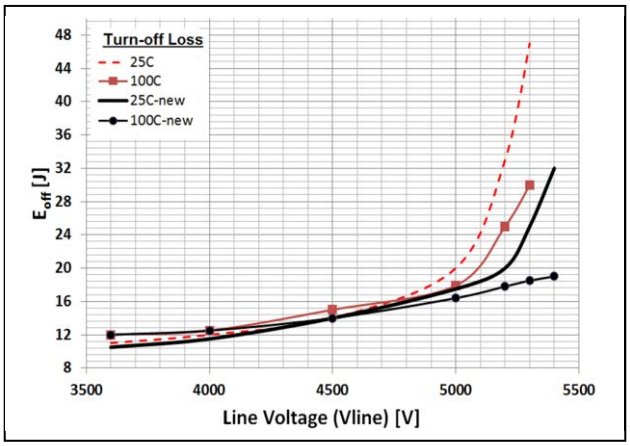


Fig.9: Comparison of measured E_{off}-Vline curves for old and new optimised modules. I_{OFF}=1000A.

5. Conclusion

In this paper we have shown the high line voltage RBSOA robustness of Dynex's 6.5kV/1000A modules. Experimental results show they can safely turn-off Ice=1000A at Vline up to 5.4kV at 25^0C and 100^0C, in an unclamped setup where no cooling was applied. The IGBT device structure has been well optmised to reduce time spent in dynamic avalanche dominated SSCM(Switching Self-Clamping Mode) before turn-off. This also means reduction in T_{doff} which is an attractive feature in HVDC and circuit breaker applications. This results in turn-off energy loss reduction of 40-50% which is important to reduce wear out and improved long term reliabiliy of the modules. The choice of buffer, collector and silicon resistivlty have been discuissed as possible parameters to consider in 6.5kV IGBT design to achieve acceptable high line voltage RBSOA. The correct choice of design parameter set will shift the Vce value at which Vline-E_{off} linearity is lost to much higher voltages without much sacrifice of Vce(sat).

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