Email: powersolutions@dynexsemi.com
Main switchboard: +44 (0)1522 500 500
Website: www.dynexsemi.com

AN6196
Gate Power Calculations
Application Note

Replaces AN6196-1
AN6196-2 February 2023 (LN42379)

When designing a gate drive to control thyristors, it is necessary to verify that the peak gate power and the average gate power will not degrade the thyristor, as well as assuring that the current pulse is of the right shape and magnitude to achieve the turn-on performance required.
[See Application Note AN4840 "Gate Triggering and the Use of Gate Characteristics"]

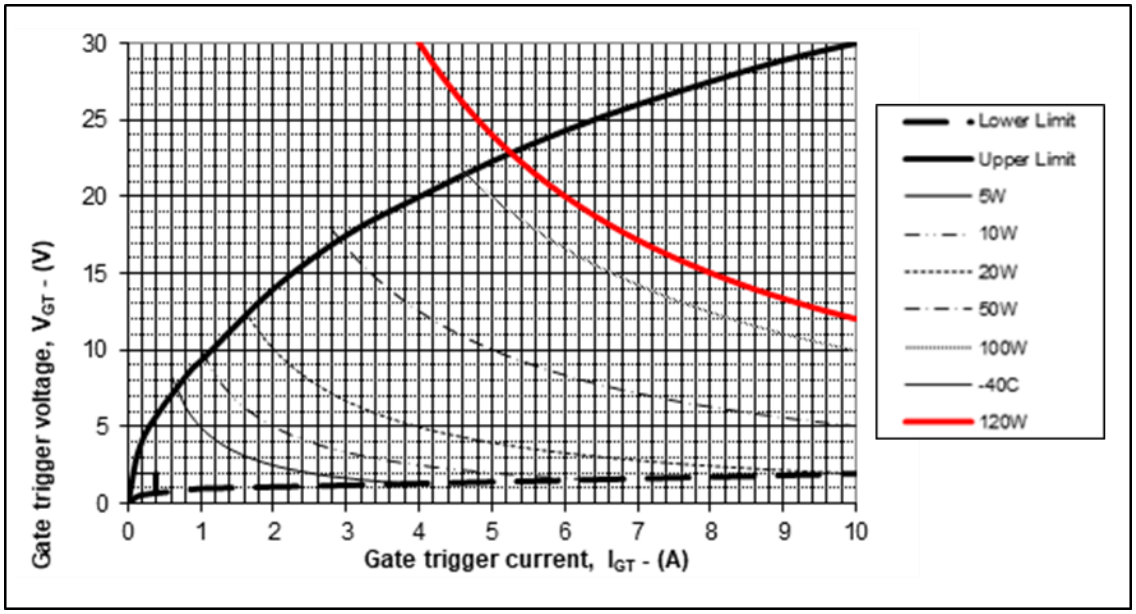
Figure 14 of Dynex i^2 thyristor datasheets contains the following table embedded in the graph.

Pulse Power P_{GM} (Watts)			
Pulse Width (µs)	Frequency (Hz)		
	50	100	400
100	150	150	150
200	150	150	125
500	150	150	50
1000	150	100	25
10000	20	-	-

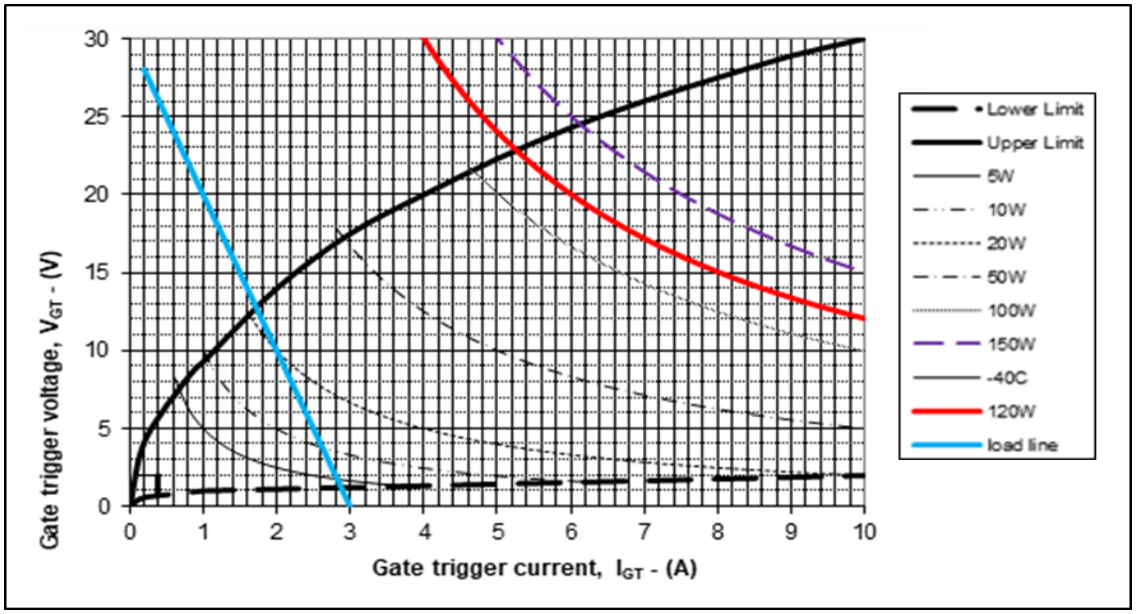
This assumes, for simplicity, that the pulses are rectangular.
The table states that the **maximum peak pulse power is 150 watts and the average power, which is Pulse Width x frequency x Pulse Power, is limited to 10 watts.**

Suppose that we have a gate drive of 12.5µs pulses with a frequency of 20kHz. This means that the maximum allowable peak gate power is 10W / (12.5E-6 x 20E3) or 40W. This would be true if the thyristor was continuously triggered by the picket fence train of pulse, but in our example the gate drive only supplies pulses for 120 electrical degrees. Thus, our equation becomes Pulse Width x frequency x Pulse Power x duty cycle ≤10W. Our maximum allowable peak (pulse) power is now 120W instead of 40W.

We can plot this on figure 15 of the datasheet.

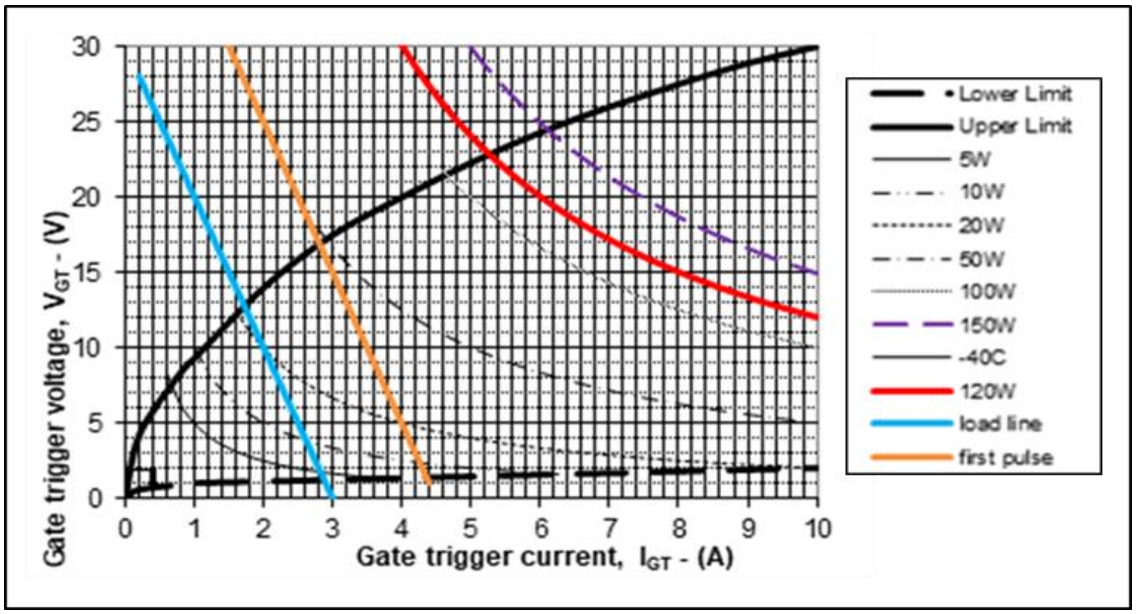


The load line of our gate drive is given by the open circuit voltage of 30V and a short circuit current of 3A. If this is plotted on the above graph it should lie to the left of the 120W peak power limit line.



Therefore, our gate drive complies with the limit of 120W when connected to our thyristor.

Because of the way our gate drive operates, the first pulse in the train is larger than the subsequent pulses because the energy reservoir capacitor does not have time to fully re-charge after the first pulse. Therefore, we must just check that the peak gate power for this initial pulse does not exceed the 150W limit. The initial open circuit voltage on the reservoir capacitor is 45V, the internal resistance is 10Ω as before so we can plot this load line too.



The load line is then compared to the 150W curve or the power calculated from the values of current and voltage where the load line intercepts the upper gate characteristic at 2.8A and 17V i.e. 48W. Either way, our initial gate pulse is less than 150W and our gate drive is fully acceptable from a gate power point of view.

Finally, a check on the magnitude of the gate current. Say the datasheet upper limit for I_{GT} in the “Gate Trigger Characteristics and Ratings” table is 350mA, then we recommend 5x I_{GT} to 10x I_{GT} as a design, or in this case 1.75A to 3.5A. From the blue load line above, we see that the intercept with the upper limit gate characteristic is just over 1.75A, so satisfactory for a reasonable di/dt performance.

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HEADQUARTERS OPERATIONS

DYNEX SEMICONDUCTOR LIMITED
Doddington Road, Lincoln, Lincolnshire, LN6 3LF
United Kingdom.
Phone: +44 (0) 1522 500500

Web: http://www.dynexsemi.com

CUSTOMER SERVICE

Phone: +44 (0) 1522 502753 / 502901

e-mail: powersolutions@dynexsemi.com